Enhanced Decoupling Current Scheme with Selective Harmonic Elimination Pulse Width Modulation for Cascaded Multilevel Inverter Based Static Synchronous Compensator

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THESIS SUBMITTED TO THE UNIVERSITY OF NOTTINGHAM
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

FEBRUARY 2015

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Abstract

This dissertation is dedicated to a comprehensive study and performance analysis of the transformer-less Multilevel Cascaded H-bridge Inverter (MCHI) based STATic synchronous COMpensator (STATCOM). Among the shunt-connected Flexible AC Transmission System (FACTS) controllers, STATCOM has shown extensive feasibility and effectiveness in solving a wide range of power quality problems. By referring to the literature reviews, MCHI with separated DC capacitors is certainly the most versatile power inverter topology for STATCOM applications. However, due to the ill-defined transfer functions, complex control schemes and formulations were emerged to achieve a low-switching frequency high-bandwidth power control. As a result, adequate controller parameters were generally obtained by using trial and error method, which were practically ineffective and time-consuming. In this dissertation, the STATCOM is controlled to provide reactive power (VAR) compensation at the Point of Common Coupling (PCC) under different loading conditions. The goal of this work is to enhance the performance of the STATCOM with the associated proposed control scheme in achieving high dynamic response, improving transient performance, and producing high-quality output voltage waveform. To evaluate the superiority of the proposed control scheme, intensive simulation studies and numerous experiments are conducted accordingly, where a very good match between the simulation results and the experimental results is achieved in all cases and documented in this dissertation.

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Acknowledgements

This work has been carried out at the Department of Electrical and Electronic Engineering in the University of Nottingham Malaysia Campus. First and foremost, I would like to express my thankfulness to my postgraduate main supervisor, Prof. Haider Abbas F Mohamed Almurib and my ex-supervisor, Dr. Mohamed S. A. Dahidah from Newcastle University, UK for their generous guidance, patience, support, and encouragement during the research work. I could not have completed this dissertation without their experiences and technical knowledge on the contents of the research work.

My gratefulness also goes to Dr. Dahidah, who dedicated a lot of time to support my work in all aspects and gave me an opportunity to collaborate with Dr. Georgios S. Konstantinou from the University of New South Wales, Australia on writing a conference paper, of which work was a part of this dissertation.

I am also grateful to my undergraduate supervisor, Prof. Mark Sumner from the University of Nottingham, who brought me to this PhD position after completion of my MEng degree in UK.

My appreciation also goes to the lab technicians, Mr. Noor Hashimi Mohamad Nor and Mr. Mohamad Irwan Mat Darus, who provided the electronic components and measuring instruments for my experimental work.

Of course, I am grateful to my family members especially my fiancée, Wendy Ng Pei Qin for their unlimited patience. Without them, this work would never come into existence.

For those who have contributed but not mentioned, please accept my thanks.

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List of Contents

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List of Figures

List of Tables

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List of Acronyms

AC	Alternating Current
AGC	Automatic Gain Controller
AI	Artificial Intelligence
APOD	Alternative Phase Opposite Disposition
BESS	Battery Energy Storage System
CB	Carrier Based
CCM	Continuous Conduction Mode
CCP	Current Clamp-on Probe
CHI	Cascaded H-bridge Inverter
CSI	Current Source Inverter
DC	Direct Current
DFT	Discrete Fourier Transform
DOL	Direct-On-Line
DSP	Digital Signal Processor
ESS	Energy Storage Systems
FACTS	Flexible AC Transmission System
FC-TCR	Fixed Capacitor, Thyristor Controlled Reactor
GCT	Gate Commutated Thyristor
GTO	Gate Turn-Off Thyristor
GUI	Graphical User Interface
HEV	Hybrid Electric Vehicle
IEGT	Injection Enhanced Gate Transistor
IGBT	Insulated-Gate Bipolar Transistor
I/O	Input/Output
IPD	In-Phase Disposition

MC	Magnetic Contactor
MCCI	Multilevel Capacitor-Clamped Inverter
MCHI	Multilevel CHI
MDCI	Multilevel Diode-Clamped Inverter
MI	Modulation Index
MPC	Model Predictive Control
MSHE	Multilevel SHE
MSS	Modified Selective Swapping
NPC	Neutral Point Clamped
OSC	OScillosCope
PCC	Point of Common Coupling
PF	Power Factor
P	Proportional
PI	Proportional Integral
PLL	Phase-Locked Loop
POD	Phase Opposite Disposition
PSO	Particle Swarm Optimization
PV	Photo-Voltaic
PWM	Pulse Width Modulation
SiC	SIlicon Carbide
SFO	Switch Frequency Optimal
SHE	Selective Harmonic Elimination
SRF	Synchronous Rotating reference Frame
STATCOM	STATic synchronous COMpensator
SVC	Static VAR Compensator
SVM	Space Vector Modulation

TCR	Thyristor Controlled Reactor
THD	Total Harmonic Distortion
TOR	Thermal Overload Relay
TSC	Thyristor Switched Capacitor
TSC-TCR	Thyristor switched capacitor, thyristor controlled reactor
TSR	Thyristor Switched Reactor
VAR	Reactive Power
VSI	Voltage Source Inverters

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List of Parameters and Variables

α	Switching angle
C_{boost}	Boost converter's filter capacitor
C_{buck}	Buck converter's filter capacitor
C_{DC}	DC-link capacitor
C_f	Coupling capacitor
C_l	Load capacitor
d	Duty cycle demand
D_O	Duty cycle of the steady-state operating point
i_c	STATCOM current
i_{cd}	STATCOM active/real/*d*-axis current
i_{cq}	STATCOM reactive/*q*-axis current
i_{cq}^*	Proposed STATCOM *q*-axis current
i_l	Load current
i_{lq}	Load reactive/*q*-axis current
i_s	Grid current
i_{sd}	Grid active/d-axis current
i_{sq}	Grid passive/q-axis current
I_C	Converter's capacitor current
I_{DC}	DC-link current
I_{DC_d}	DC-link active/real/*d*-axis current
I_{DC_q}	DC-link reactive/*q*-axis current

I_L	Converter's inductor current
f	Grid fundamental frequency
f_s	Sampling frequency
f_{c_boost}	Boost converter cut-off frequency
f_{c_buck}	Buck converter cut-off frequency
f_{sw}	Inverter switching frequency
f_{sw_boost}	Boost converter switching frequency
f_{sw_buck}	Buck converter switching frequency
k	Sample period
K	K factor
K_{p_id}	Gain of P-controller for *d*-axis current vector controller
K_{p_iq}	Gain of P-controller for *q*-axis current vector controller
K_{p_vd}	Gain of P-controller for *d*-axis voltage vector controller
L_{boost}	Boost converter's filter inductor
L_{buck}	Buck converter's filter inductor
L_f	Coupling inductor
L_l	Load inductor
L_s	Grid inductor
m_i	Modulation index
M	Total units of H-bridge inverter per phase-leg
N	Total switching angles per quarter cycle
M_N	Number of voltage-levels
P_c	STATCOM active/real/*d*-axis power

P_l	Load active/real/*d*-axis active power
Q_c	STATCOM reactive/*q*-axis power
Q_l	Load reactive/*q*-axis power
R_{boost}	Boost converter's filter resistor
R_{buck}	Buck converter's filter resistor
R_f	Coupling resistor
R_l	Load resistor
R_s	Grid resistor
S_c	STATCOM apparent power
S_l	Load apparent power
T_{id}	Time rate of *d*-axis current vector controller
T_{iq}	Time rate of *q*-axis current vector controller
T_{vd}	Time rate of *d*-axis voltage vector controller
v_c	STATCOM voltage
v_{cd}	STATCOM active/real/*d*-axis voltage
v_{cq}	STATCOM reactive/*q*-axis voltage
v_c^*	Resultant STATCOM voltage
v_{cd}^*	Resultant STATCOM active/real/*d*-axis voltage
v_{cq}^*	Resultant STATCOM reactive/*q*-axis voltage
v_{cc}^*	Resultant STATCOM voltage of an operating point
v_{ccd}^*	Resultant STATCOM active/real/*d*-axis voltage of an operating point

v_{ccq}^{*}	Resultant STATCOM reactive/*q*-axis voltage of an operating point
v_L	Voltage drop across L_f
v_{pcc}	Grid voltage
v_{pccd}	Grid active/real/*d*-axis voltage
v_{pccq}	Grid reactive/*q*-axis voltage
V_{DC}	Total DC-link voltage
V_{DC_d}	DC-link active/real/*d*-axis voltage
V_{DC_q}	DC-link reactive/*q*-axis voltage
$V_{DC\_d}^{*}$	Resultant DC-link active/real/*d*-axis voltage
V_{DC_max}	Maximum DC-link voltage
V_{DC_min}	Minimum DC-link voltage
V_{SO}	DC voltage source
ω	Grid angular frequency
ω_{cross_boost}	Boost converter's crossover frequency
ω_{cross_buck}	Buck converter's crossover frequency
ω_{p_boost}	Boost converter's pole-frequency
ω_{p_buck}	Buck converter's pole-frequency
ω_{z_boost}	Boost converter's zero-frequency
ω_{z_buck}	Buck converter's zero-frequency
Z_f	Coupling impedance
δ	Phase difference between v_{pcc} and v_c

φ	Phase difference between v_{pcc} and i_c (i.e., PF angle)
θ	Phase angle of v_{pcc}

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Chapter 1 Introduction

The penetration of renewable energy and increased capacity of distributed generations have introduced power quality and efficiency issues to the modern power networks due to unmanaged power flow. These include low-power factor (PF), voltage disturbances, excessive harmonics as well as voltages and/or currents unbalance. Reactive loads, which naturally possess low-PF, draw excessive VAR restricting the maximum active power transfer and moreover, adding losses to power transmission and distribution systems [1]. Voltage disturbances (i.e., sags, swells, transients, and variations) which are caused by low-PF loads and sudden fluctuation of the load, contribute to the failure of electronic components causing malfunction of modern process control and undesired trips [2]-[3]. In addition, the unbalanced power flow which are caused by uneven distribution of single-phase loads over the phases, induces additional losses to the electrical equipment restricting their tolerance in terms of reliability and stability (i.e., shorter lifespan) [4]-[5].

In recent years, electrical and electronic equipment have become ever more technically advanced; in many cases, followed by increased voltage sag susceptibility. As a result, there are more interruptions in the production phase with an increased power quality related costs. Therefore, it is essential to improve the voltage stability of the utility power network systems under both contingency and normal operating conditions [6].

The aforementioned phenomena arising from unmanaged power flow appear to be more significant in weak power system where the grid impedance is relatively high [3]. Generally, by controlling the reactive current, these problems can be minimized or even fully eliminated. In the past few decades, the rapid growth in power electronics industry has opened up opportunities for improving the operation and management of the utility power network systems [7]. This led to the development of FACTS controllers, such as VAR compensators, to enhance neighbouring utilities and regions into more economical and reliable exchange of power [8]-[9]. Particularly, the development of shunt-connected STATCOM has played a major role in FACTS.

The conventional three-level six-pulse voltage source inverters (VSIs) based STATCOM have proven their effectiveness, practicality, and superiority over the traditional shunt-connected compensators to provide harmonic elimination, VAR compensation, and voltage regulation features [26]. One reason for these is because it has no mechanical inertia (i.e., like a synchronous machine). Thus, STATCOM can provide quicker response to the changing conditions in the power system, which can theoretically go from full lag to full lead in a few cycles [10]-[11]. In addition, STATCOM integrated with Energy Storage Systems (ESS) has wider adjustable active current range to provide support for applications that require heavy active current compensation. For these reasons, many industries have started to employ STATCOM in their power network for power quality improvements and long term cost savings [12]-[24]. Appendix A shows the list of STATCOM installations in operation and under construction across the world.

Multilevel inverters have proven their ability to overcome the problems associated with the conventional VSIs; therefore, received an extensive research over the last few decays [25]-[28]. There are various multilevel inverter topologies that have been proposed and reported in the open literature [29]. Among all these, MCHI has been an attractive topology for STATCOM system due to its modularization, extensibility, control simplicity, and the ability to provide negative sequence current compensation [30]. The structure of MCHI is simply formed by connecting several H-bridge inverters with separated DC sources in series to produce a multilevel staircase waveform which is virtually sinusoidal as the number of level increases [31]-[59].

On the other hand, the choice of modulation technique plays an important role in STATCOM systems as it has a high impact on the compensation objectives, transient, as well as steady-state performances. Therefore, several multilevel PWM techniques have been investigated, proposed, and documented in the literature including CB-PWM [62]-[66], space vector modulation (SVM) [66]-[79] and MSHE-PWM [80]-[99]. Among these techniques, MSHE-PWM offers a tight control of the low-order harmonics with considerable low-equivalent switching frequency; therefore, leading to low-switching power loss and good harmonic performance. Thus, it

is considered a competitive solution for medium- and high-power conversion systems such as STATCOM and other utility based inverters.

Furthermore, the selection of appropriate control scheme is an essential factor which defines the performance of a STATCOM system as well as its ability to detect and response to power exchange demands with high precision and speed. Several control schemes of MCHI based STATCOM have been implemented for reactive current compensation and voltage regulation by using either frequency- or time-domain approach to meet the predefined performance requirements [156]. Most recent algorithm development adopts time-domain approach due to its ability to compute the reference currents and precisely traces the load changes almost instantaneously. The well-known *abc*-to-*dq* transformation or else known as Synchronous Rotating reference Frame (SRF), which incorporates decoupling feed-forward/feedback systems with appropriate control algorithms, is commonly used to achieve lower steady-state errors and acceptable transient characteristics in response to a step change of the loading conditions.

The next section briefly introduces several types of FACTS controllers.

1.1 FACTS and Shunt-connected Controllers

The concept and development of FACTS technology were pioneered by N. G. Hingornani and L. Gyugyi in late 1980s [100]-[102] to enhance the value of electrical energy [10]. The term “FACTS” covers a whole range of power electronic controllers and has been defined by IEEE as [1]:

“A power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability.”

FACTS controllers offer various functions such as [10]:

i) Contributing to emergency control by avoiding cascading outages;

ii) Damping of oscillations to improve power system stability;

iii) Regulating the power flows and providing VAR support to prevent of voltage collapse;

iv) Secure loading of transmission lines near their thermal limits.

Generally, these controllers are categorized as following:

a) Series controllers (see Figure 1-1(a)): Inject voltage in series with the line either by variable series impedance multiplied with the current flow through it or by power electronics based variable source.

b) Shunt controllers (see Figure 1-1(b)): Inject current into the power system at the PCC either by variable shunt impedance connected to the line voltage or by power electronics based variable source, or both.

c) Combined series-series controllers (see Figure 1-1(c)): Provide independent series VAR compensation for each line and also transfers real power among the lines via the DC power link.

d) Combined series-shunt controllers (see Figure 1-1(d)): Inject current and voltage into the power system via the shunt and series parts of the controller, respectively. Real current can be exchanged between the controllers via the DC power link.

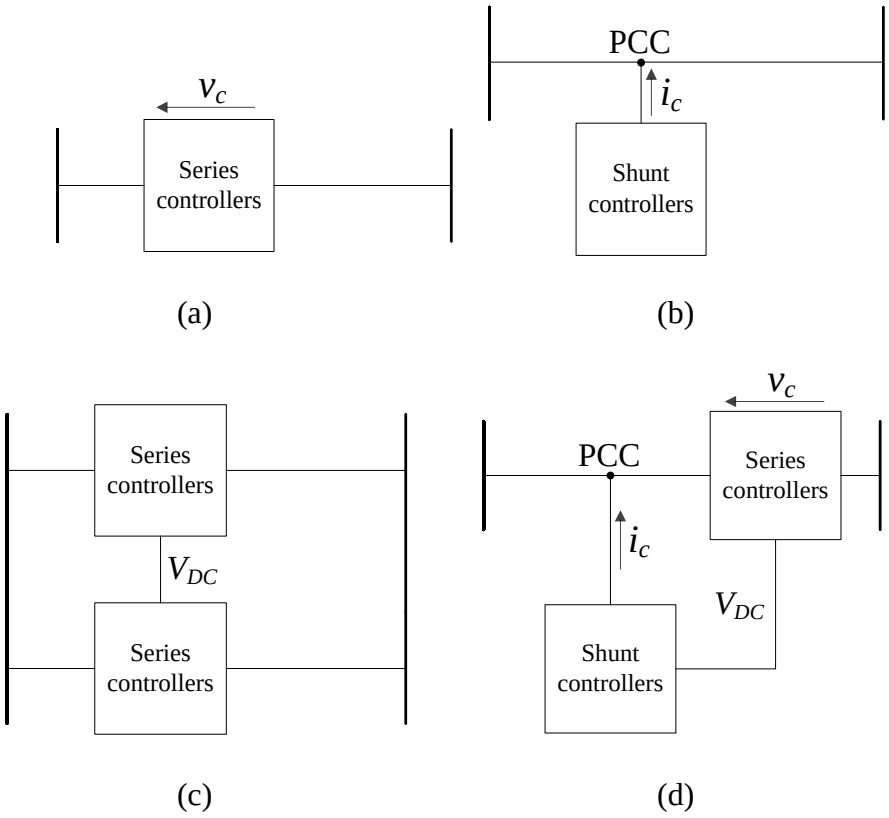

Figure 1-1. Types of FACTS controllers: (a) series controller, (b) shunt controller, (c) combined series-series controller, and (d) combined series-shunt controller.

Among those controllers, shunt controllers are the most cost-effective choice for compensating VAR and harmonics with satisfactory voltage profile in the existing transmission lines [103]. They have been recognized in enhancing the system's transient stability as well as damping the power oscillations at a substation bus/PCC by injecting a combination of active and reactive currents [10].

For these reasons, the next subsections address on the functions of shunt-connected FACTS controllers.

1.1.1 First Generation of Shunt-Connected FACTS Controllers

The first generation of shunt-connected FACTS controllers provides the required reactive current into the power system through variable reactive impedance controlled by thyristor switches [10], [104]. This variable impedance is formed by the combination of traditional capacitor and inductor/reactor banks. As long as the injected reactive current is in phase quadrature with the grid voltage, these controllers only consume or supply variable reactive current. Particularly, the shunt-connected inductors are applied to minimize the transmission lines' overvoltage during light load conditions, whereas under heavy load conditions, shunt-connected capacitors are employed to maintain the grid voltage-levels closed to its rated value. Some of the first generation shunt-connected FACTS controllers are [10]:

a) Thyristor Controlled Reactor (TCR) (see Figure 1-2(a)): The effective reactance of a fixed inductor is continuously varied by partial conduction of the bidirectional thyristor valve with firing delay angle control.

b) Thyristor Switched Reactor (TSR) (see Figure 1-2(a)): The effective reactance of a fixed inductor is varied in steps by full- or zero-conduction operation of the bidirectional thyristor valve.

c) Fixed Capacitor, Thyristor Controlled Reactor (FC-TCR) (see Figure 1-2(b)): The constant capacitive VAR generation of the fixed capacitor is opposed by the variable VAR absorption of the TCR to produce the required VAR output.

d) Thyristor Switched Capacitor (TSC) (see Figure 1-2(c)): The effective reactance of a fixed capacitor is varied in steps by fully open or close the bidirectional thyristor valve. A current limiter is usually employed to limit the surge current in the thyristor valve when the transient free switching conditions are not satisfied (i.e. capacitor residual voltage and the applied AC voltage are not equal).

e) Thyristor Switched Capacitor, Thyristor Controlled Reactor (TSC-TCR) (see Figure 1-2(d)): Consists of a number of TSC branches to approximate the VAR demand along with a TCR device to cancel the surplus capacitive VAR.

f) Static VAR Compensator (SVC): A combination of TCR, TSR, and/or TSC whose output is adjusted to exchange capacitive or inductive current so as to control specific parameters of the power system, typically the grid voltage.

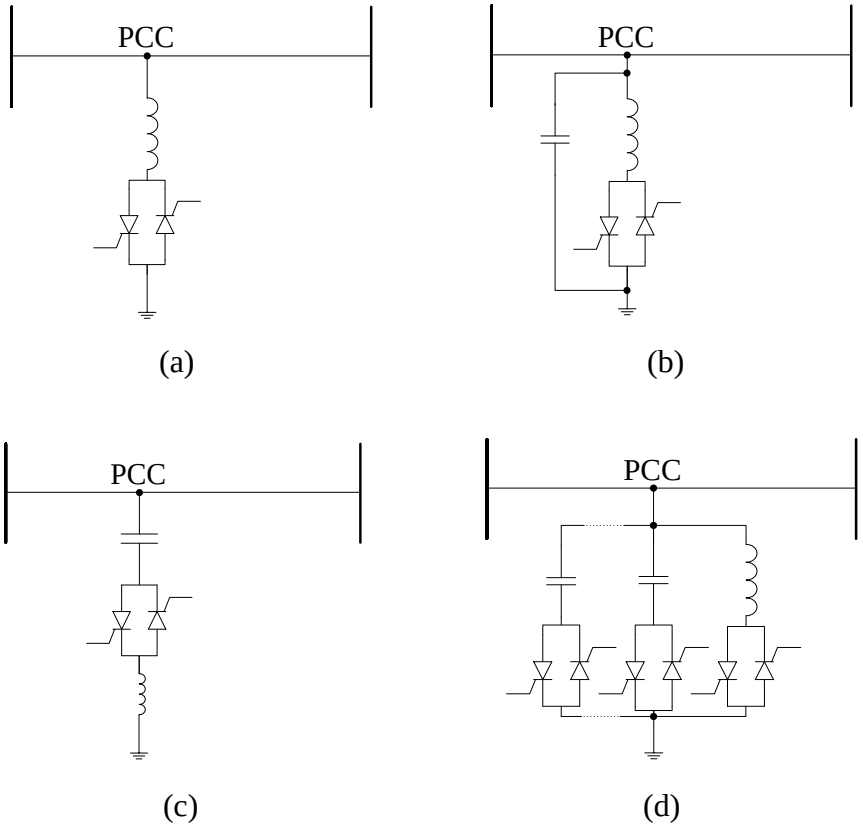

Figure 1-2. Shunt-connected controllers: (a) TCR or TSR, (b) FC-TCR, (c) (TSC), and (d) TSC-TCR or SVC.

Due to the slow response of switching capacitors, the SVC would not be able to timely trace the fast changing reactive current reference unless the rate of change is very low (i.e., hundreds of fundamental cycles and above [10]). Nevertheless, the presence of high-power semiconductors with gate turn-off capability has led to the possibility of generating controllable reactive directly by various power electronics switching inverters [9].

The next subsection addresses the functions and benefits of the static inverters based shunt-connected FACTS controllers.

1.1.2 Second Generation of Shunt-Connected FACTS Controllers

The second generation of shunt-connected FACTS controllers is based on high-power static inverter, which controls the current with the connected network to provide the common compensation characteristic of the former. Hence, these shunt controllers substantially lower the rating requirement of the passive elements (i.e., capacitors and inductors) and active components (i.e., diodes and switches) compared to the conventional variable impedance controllers. STATCOM (see Figure 1-3) is an advanced version of SVC which consists of a PWM switching inverter with capacitor connected at the DC-link. Its AC output voltage is continuously adjusted based on the reactive current demand such that the required reactive current is flowing to the power system through the coupling inductor or transformer.

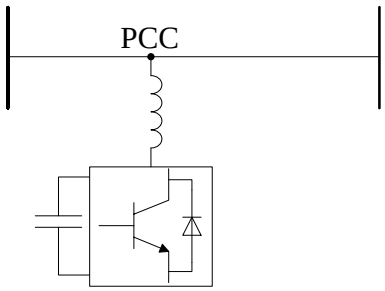

Figure 1-3. Single-line diagram of VSI based STATCOM.

The STATCOM offers several advantages compared with the SVC of the same power ratings. This includes [10], [105]-[108]:

i) Ability to maintain and operate across its full output current range (i.e. from maximum capacitive to maximum inductive output current) even

at low AC system voltage (i.e., typically about 0.2 p.u. at which the inverter still would be able to absorb the necessary real current from the AC system to supply its operating losses) [10];

ii) Attain short time overload capability (i.e., over 200%) with proper choice of thermal and design ratings [109]-[110];

iii) Capability to exchange real power for enhancing dynamic compensation, improving power system efficiency, and preventing power outages;

iv) Faster response time and greater control transient stability margin;

v) Significant size reduction due to reduce number of passive elements, hence, less construction cost.

The next subsection briefs the operating principals of the shunt-connected STATCOM.

1.1.2.1 Operating Principals of the STATCOM

Figure 1-4 illustrates a single-line block diagram of the STATCOM which is shunted to the power system via a coupling inductor Z_f or a tie reactance, which in practical is provided by the per phase leakage inductance of the coupling transformer, at the PCC [10]. The STATCOM itself consists of a self-commutated VSI in addition to the control circuit and ESS.

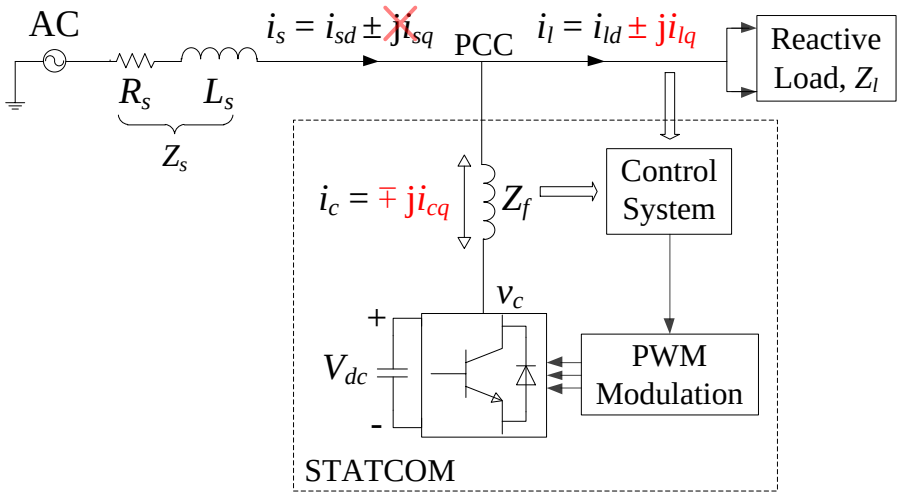

Figure 1-4. Key component of a typical STATCOM system.

Details regarding the total harmonic distortion (THD) of the STATCOM output current i_c and its dynamic response with respect to the size of the inductor (i.e., inductance) and the operating range of the inverter were demonstrated by Kumar in [111]. It was concluded that for a given output current and operating voltage, the minimum size of the coupling inductor is decided by the STATCOM output current THD while the maximum inductance is limited by the operating range of the inverter as well as the cost. Besides that, extensive reviews regarding on the influence of PWM parameters (i.e., switching frequency) and amplitude modulation ratio on the coupling transformer's iron losses were presented by Boglietti et al. [112], Liu et al. [113], as well as Deepthi and Saxena [114]. These studies concluded that the amplitude modulation ratio plays an important role in the iron loss while the effect of switching frequency on the iron loss is negligible. The reason is that at a higher amplitude modulation ratio, the amplitude of the harmonic components becomes relatively low; therefore, reducing the iron loss.

Figure 1-5 depicts a single-phase equivalent circuit of the STATCOM, where v_{pcc} is the grid voltage; i_c and v_c are the STATCOM's current and voltage, respectively.

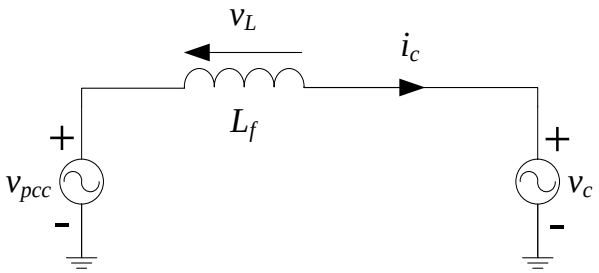

Figure 1-5. Single-phase equivalent circuit of the STATCOM.

By controlling the amplitude of v_c and its phase angle with respect to v_{pcc}, one can control the real and reactive current exchange between the power system and the STATCOM through the coupling inductor. For instance, when v_c exceeds v_{pcc}, the STATCOM is operating in capacitive mode and supplies reactive current to the PCC. Conversely, the STATCOM is operating in inductive mode and draws reactive current from the PCC whenever v_c is lower than v_{pcc}. This is clearly illustrated by the phasor diagram of Figure 1-6, where v_c and v_{pcc} are controlled to be in-phase for pure reactive current exchanges.

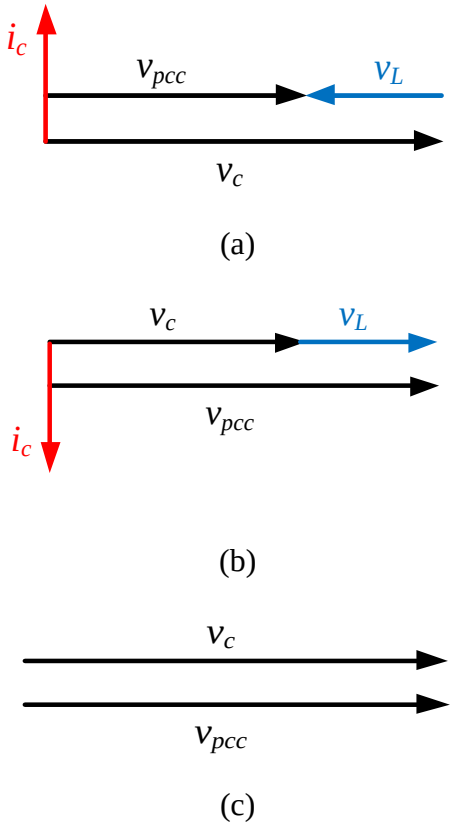

Figure 1-6. Phasor diagram of STATCOM operating in (a) capacitive, (b) inductive, and (c) floating mode.

However, if v_c is equal and in-phase to v_{pcc}, the STATCOM is operating in floating mode and there is no exchange of active and/or reactive currents (see Figure 1-6(c)). On the other hand, if v_c lags v_{pcc} by an angle δ, active current will be absorbed by the STATCOM and when v_c leads v_{pcc}, the STATCOM delivers active current to the PCC.

Figure 1-7 depicts the steady-state four quadrants operating range of the STATCOM in the PQ plane, where the active and reactive variables are defined in cosine and sine functions, respectively. The conventional STATCOM, which incorporates a VSI with a DC-link capacitor, has only two steady-state operating modes. These modes are resided in quadrant I (i.e., capacitive mode) and quadrant III (i.e., inductive mode) of the phasor diagram depicted in Figure 1-7. However, for the STATCOM integrated with Battery Energy Storage System (BESS), the steady-state operating modes can be expanded and equally operated in all four quadrants [35].

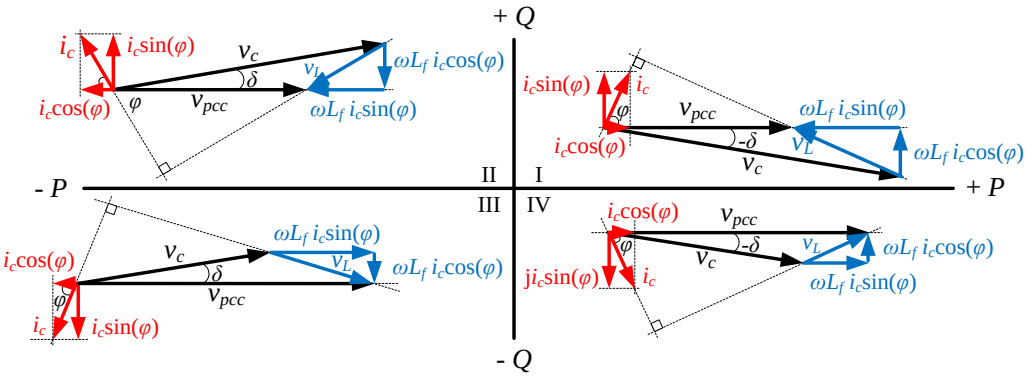

Figure 1-7. Four-quadrant operation of STATCOM.

Equation (1-1) defines the amount of active and reactive current exchange through the coupling inductor as follows:

$$i_c = \frac{v_{pcc} - v_c \angle \delta}{Z_f} = i_c \angle \varphi = \pm i_c \cos(\theta) \pm j i_c \sin(\theta) = \pm i_{cd} \pm j i_{cq} \tag{1-1}$$

where δ is the phase difference between v_{pcc} and v_c, Z_f is the coupling impedance, φ (i.e., PF angle) is the phase difference between i_c and v_{pcc}, i_{cd} is the active or real current used to charge and discharge the DC-link storing devices, and i_{cq} is the reactive current flowing through L_f.

Based on (1-1) the amount of apparent, active, and VAR exchange between the power system and the STATCOM are defined by (1-2), (1-3) and (1-4), respectively.

$$S_c = v_{pcc} i_c \tag{1-2}$$

$$P_c = v_{pccd} i_{cd} - v_{pccq} i_{cq} \tag{1-3}$$

$$Q_c = v_{pccd} i_{cq} + v_{pccq} i_{cd} \tag{1-4}$$

where v_{pccd} and v_{pccq} define the *d*-axis and *q*-axis grid voltage, respectively.

From Figure 1-4, VSI is an essential part for the STATCOM system [115]-[117]. The conventional VSI based STATCOM is started off with two-level inverter, or else known as six-pulse inverter in three phase systems,

employing turn-off capability semiconductor devices. However, there are several problems associated with this configuration. This includes multi-pulse inverters which are structured by cascading multiple six-pulse inverters through different configurations of transformer connections in an effort to enhance harmonic performance and increase the output power [118]-[121]. These transformers are uneconomical and contribute to more than half (i.e. about 70%) of the total losses of the system [155]. Moreover, they are very bulky and unreliable due to magnetizing and surge overvoltage problems caused by saturation of the transformers in transient states [24].

With the rapid development of power semiconductor technologies, multilevel VSI topologies are proven to be more superior over the conventional counterpart in a wide range of applications, especially FACTS technology. Many novel multilevel inverter topologies are realized and patented, along with plentiful modulation techniques and control schemes, which have been developed to cater for different STATCOM applications and performance requirements. However, among all the multilevel inverter topologies, MCHI with separated DC capacitors is recognized to be the most feasible topology for many reasons in VAR compensation.

The next section reviews the employment of MCHI topology in STATCOM systems.

1.2 Review of Multilevel Cascaded H-bridge Inverter Based STATCOM

The concept of MCHI was employed to STATCOM system for the first time in 1997 [24], [31]. Since then, more research and development on this topology have been carried out from low-power applications, such as electric vehicles, to very high-power applications, such as adjustable-speed drive applications and FACTS controllers. Basically, MCHI synthesizes its phase voltage by adding and subtracting the voltage-levels produced from each H-bridge inverter [26]. By simply stacking of more H-bridge inverters, high-number of output voltage-levels with good harmonic performance can be achieved by switching the power semiconductor devices at the fundamental frequency only. This naturally minimizes the entire system losses and moreover, alleviates the necessity of coupling transformer and higher-order

(i.e., large size) output filter [27]. Furthermore, a three-phase MCHI topology, which composed of three identical phase-legs of series-connected H-bridge inverters, can generate different output voltage waveforms to compensate and rebalance the reactive currents in a three-phase network. All these features, therefore, make the MCHI a promising topology compared to others in modern FACTS technology [28]-[30].

To date, the combination of MCHI topology and STATCOM concept remains as an interesting topic for researchers to enhance its dynamic and transient performances using different control schemes [31]-[59]. Generally, a complete STATCOM controller consists of external, internal, and gate control. Same as other inverter topologies, MCHI comprises a great number of gate-controlled semiconductor switches. The gating commands for these switches are generated by the internal controller in response to the real and/or VAR reference signals provided by the external controller. Thus, in order to achieve a stable and efficient operation of STATCOM, an adequate mathematical model of these controllers is required to define and optimize their parameters. Furthermore, it is worth noting that a STATCOM is required to response and reached steady-state within 200ms according to the grid codes [122].

Another challenge associated with MCHI topology is choosing a modulation technique which is capable of producing good quality waveforms with minimum filtering and a low-switching frequency. The low-switching frequency of the devices is important since for a high power inverter, the switching losses of the power semiconductor devices will contribute significantly to power losses in the inverter; therefore reducing its efficiency [60]. For instance, an interesting comparison between the switching frequency (i.e., ranging from 1 kHz to 12 kHz) and the IGBT inverter was demonstrated by Malfait et al. [61]. It was concluded that the inverter loss reaches a minimum around a frequency of 3 kHz.

1.3 Problem Statements

Generally, there are significant trade-off between the integral function, dynamic response, and steady-state error (i.e., transient performance) when considering a PI controller in a control system. For instance, with high integral

gain, zero steady-state error can be achieved but at the expenses of poor dynamic response. However, when it comes to multilevel inverter, simply stacking more H-bridge inverters will achieve high bandwidth and good harmonic performance; therefore, fundamental (i.e., low) switching frequency as well as low integral gain can be employed to achieve a satisfactory dynamic response and low steady-state error. In addition, the use of MCHI enabling the elimination of bulky, heavy, and costly line frequency transformer [42], [153]-[154], which contributes to almost 70% of the total power losses per a MVA rating [155].

In the past two decades, numerous control schemes have been applied to the MCHI based STATCOM with a particular emphasis on the dynamic and transient responses in providing VAR compensation [24]-[59]. In most cases, the Proportional Integral (PI) controllers have been considered as the simplest way to perform control actions in the feedback loops. However, several works have revealed that the PI-controllers could not provide precise tracking of the command values [9] due to the variations of parameters and operating points [40], [45] that leads to poor transient response and instability of the STATCOM system [48]. Moreover, methods to remedy the issues involve high-switching frequency (i.e., 5 kHz [154], 10 kHz [9], 12 kHz [55] and [185]) to attain the desired current loop bandwidth as well as complicated rules and factors to relate the input variables to the output model properties [45]-[46]. Besides that, the controller's parameters (i.e., gain parameters) were not specifically defined [31]-[33] and moreover, details on the modulation technique as well as the employment of both the sampling and switching frequencies are not discussed. In addition, a high-number of levels increases the control complexity and introduces voltage imbalance problems [42], [45], [46]; therefore, complex formulations of the external controller come at the expenses of increased computational burden of Digital Signal Processor (DSP) as well as deteriorating the reliability and stability performance of the overall control system.

On the other hand, conventional MSHE-PWM technique with equal DC voltage-levels is usually selected to eliminate the defined low-order harmonics with limited switching frequency and thus, to avoid the steady-state resonance. However, when the transient event occurs, the SHE has limited

capability to damp the resonance due to the time delay in real-time implementation [50]-[51].

1.4 Objectives of the Dissertation

The aim of this dissertation is to present the modelling of MCHI based STATCOM for compensating the VAR at the PCC, along with the proposed new reactive current reference algorithm (i.e., i_{cq}^{*}) that enables simple decoupling feed-forward current control design (i.e., the proposed control scheme). The decoupling feed-forward current controller provides instantaneous response without using any integral function and filtering circuit, while utilizing the proposed i_{cq}^{*} algorithm to minimize the steady-state error of the response in order to achieve closed loop transient response enhancement and low settling time (i.e., shorter response and oscillation period). For instance, instead of adjusting the PI coefficients of the controllers to attain good transient response for a particular system changes or loading condition [29], the proposed i_{cq}^{*} algorithm utilized the availability of variables, which is the grid v_{pcc} and STATCOM voltage v_c, to achieve that without sacrificing the dynamic performance. In addition, the proposed control scheme can be equally applied irrespective of the number of levels under any loading conditions.

Besides that, this dissertation exploits the feature of the newly developed MSHE-PWM technique into the proposed STATCOM system [98]. The proposed MSHE-PWM method increases the degree of freedoms in the formulation with variant DC voltage-levels and hence, the number of harmonics to be eliminated with relatively low-switching frequency (i.e., 1.6 kHz); therefore, leading to better harmonic profile and wider inverter's bandwidth. It could also find the solution of the constant switching angles for a much wider range of Modulation Index (MI) when compared with the fixed DC voltage-levels case. Furthermore, the method provides constant switching angles and linear pattern of DC voltage-levels over the full range of the m_i, which in turns eliminates the tedious steps and eases the implementation of the MSHE-PWM for dynamic systems such as STATCOM. All these advantageous are illustrated in the chapters that follow.

The main objectives of this research are:

i) To study and understand the working concepts and theories of STATCOM to line integration and develop simulation circuits to assimilate the real STATCOM;

ii) To develop a control scheme for VAR compensation, taking into consideration the response time and the compensation accuracy;

iii) To introduce MCHI with the MSHE-PWM technique to overcome the limitations of the conventional inverters and modulation techniques for STATCOM to grid application systems. The work minimizes the total harmonic distortion of the inverter output as well as the inverter losses;

iv) To validate the effectiveness of the proposed control algorithms/scheme with a scaled down laboratory prototype in providing VAR compensation and PF correction.

1.5 Dissertation Contributions

The key contributions of this work are summarized as follows:

i) This dissertation presents an overview of the most widely used FACTS controllers, inverter topologies, and modulation techniques. The recent developed of control schemes for MCHI based STATCOM system are also analysed;

ii) This dissertation proposes a generalized formulation for the decoupling feed-forward current controller to accurately attain the controller parameters;

iii) This dissertation proposes a novel, simple, intuitive, and practical reactive current reference algorithm (i.e., i_{cq}^{*}) incorporated with the decoupling feed-forward current controller (i.e., the proposed control scheme) to enhance the transient response and steady-state error without an integral function in the feedback loop;

iv) This dissertation extends the application of the proposed control scheme to MCHI combined with equal and variant DC voltage-levels;

v) This dissertation extends the newly developed MSHE-PWM with variable DC voltage-levels technique to MCHI based STATCOM system controlled by the proposed control scheme;

vi) The implementation of the voltage closed loop controllers is presented for DC-DC buck- and boost-type converters;

vii) This dissertation presents the detailed modelling of the STATCOM with its associated proposed control scheme using Matlab/Simulink;

viii) This dissertation provides experimental verification to support the simulation findings as well as the ruggedness of the proposed control scheme.

1.6 List of Publications

The following papers were published with material directly relating to this dissertation:

1.6.1 Journals

i) K. H. Law, M. S. A. Dahidah, and H. A. F. Almurib, "SHE-PWM cascaded multilevel inverter with adjustable DC-voltage levels control for STATCOM applications", *IEEE Transaction on Power Electronics*, vol. 29, no. 12, pp. 6433-6444, Dec. 2014 [Impact Factor: 4.08]

ii) K. H. Law, M. S. A. Dahidah, and H. A. F. Almurib, "A new reactive current reference algorithm for STATCOM system based on cascaded multilevel inverters", *IEEE Transaction on Power Electronics*, DOI: 10.1109/TPEL.2014.2341318 [Impact Factor: 4.08]

1.6.2 Conference Papers

i) K. H. Law, M. S. A. Dahidah, and N. Marium, "Cascaded multilevel inverter based STATCOM with power factor correction feature", in *IEEE Conference on Sustainable Utilization and Development in Engineering and Technology*, Oct. 2011, pp. 1-7.

ii) K. H. Law, M. S. A. Dahidah, G. S. Konstantinou, and V. G. Agelidis, "SHE-PWM cascaded multilevel converter with adjustable DC sources control for STATCOM applications", in *IEEE 7th International Power Electronics and Motion Control Conference*, Jun. 2012, pp. 330-334.

iii) K. H. Law and M. S. A. Dahidah, "DC-DC boost converter based SHE-PWM cascaded multilevel inverter control for STATCOM systems", in *IEEE International Power Electronics Conference*, May 2014, pp. 1283-1290.

iv) K. H. Law and M. S. A. Dahidah, "New current control algorithm for STATCOM operation under unbalanced condition employing multilevel SHE-PWM approach", in *IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems*, Jun. 2014, pp. 1-7.

1.7 Dissertation Outline

The dissertation is organized as follows:

Chapter 2 presents the fundamental concepts associated with the VSI based STATCOM including an overview of various configurations of multilevel VSIs. Since the fundamental focus of this dissertation is on MCHI based STATCOM, therefore, the common multilevel PWM techniques and control schemes for harmonic and VAR compensation are also documented in this chapter.

Chapter 3 presents the mathematical derivation of the proposed control scheme with power decoupling capability to enhance the transient response of five-level CHI based STATCOM during the steady-state condition. The modelling of conventional CB-PWM technique is presented in this chapter as well. Selected simulation and experimentally validated results confirming the proposed control scheme are reported and thoroughly discussed.

Chapter 4 present the new MSHE-PWM with variable DC voltage-levels technique based STATCOM employing five-level CHI configuration controlled by the proposed control scheme. For simplicity, DC-DC converters with closed loop voltage control are utilized to provide variable DC voltage-

levels required by each H-bridge inverter level. Their mathematical models derivation is also reported in the chapter. Analysis as well as simulation and experimental results highlighting the inherent advantages of the new technique are presented as well through a comparison with the former conventional CB-PWM technique.

Chapter 5 extends the newly developed MSHE-PWM technique and the proposed control scheme based STATCOM to the unbalanced three-phase AC system. The proposed control scheme based SRF along with its implementation to regulate as well as balance the grid voltages and currents are also demonstrated in this chapter. Only simulation results are presented to illustrate its enhanced characteristics.

Chapter 6 gives the conclusions and future research directions for the work followed by several appendices containing information on the derivation of controllers and associated analysis.

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Chapter 2 Literature Review

2.1 Introduction

This chapter focuses on the operation principal of STATCOM system with more attention to the development of VSI topologies. Both conventional two-level inverters and multilevel inverters are discussed; highlighting the inherent advantages and disadvantages of each one. The chapter also presents the most commonly used modulation techniques for VSIs such as CB-PWM, SVM, and MSHE-PWM techniques. A particular consideration is also given to the control schemes of STATCOM as it forms the core subject of this dissertation. Numerous literatures were reviewed and studied covering the most recently developed and published methods.

Chapter 2 is organized as follows: Section 2.2 describes the VSI technology along with the common inverter switching techniques and control schemes for VAR and/or harmonic compensation. Finally, the chapter is a summarized in Section 2.3.

The next section presents the circuit configurations of STATCOM system.

2.2 Key components of STATCOM System

The STATCOM system has generally three main sub-systems or components which are categorized as follows:

i) Self-commutated inverter (see Section 2.2.1) that consists of power semiconductors and energy storage devices and controlled to absorb and deliver power from/to the AC system;

ii) Coupling inductor which interfaces the STATCOM with the power system as well as reduces the harmonic currents;

iii) Control scheme (see Section 2.2.2) which performs feed-forward/feedback control according to the measured variables and the command signals as well as produces PWM switching signals to drive the power inverter.

Although the focus of this dissertation is on the MCHI control schemes, for completeness, a brief review on the most widely applied inverter topologies, (i.e., conventional, diode- and capacitor-clamped) and modulation techniques (i.e., CB-PWM, SVM, and SHE-PWM) are also included. An intensive survey on the feed-forward/feedback control schemes based on *dq*-method is presented in a separate section later in this chapter.

2.2.1 Self-commutated Inverters

2.2.1.1 Conventional Inverters

Conventional single-phase (i.e., H-Bridge) or three-phase (i.e., six-pulse) inverters are usually referred to as two- and three-level inverters. These inverters generate the required AC waveform from a DC voltage (i.e., batteries, capacitors, etc.) and capable to transfer power in either direction. There are two basic categories of such inverters [10]:

i) Current Source Inverter (CSI) (see Figure 2-1(a)) uses inductive energy storage as a DC current source, in which DC current flow always has one polarity and the power reversal takes place through reversal of DC voltage polarity;

ii) VSI (see Figure 2-1(b)) uses capacitive energy storage as a DC voltage source, in which DC voltage always has one polarity and the power reversal takes place through reversal of DC current polarity.

However, VSI is often favoured over CSI as the building block of STATCOM due to the following reasons [10]:

i) Current source termination by a current charged inductor is much lossier than the voltage source termination by a voltage charged capacitor;

ii) CSI requires additional capacitive filter C_f for voltage source termination, whereas VSI has a natural current source termination which is provided by the leakage inductance of the coupling transformer;

iii) Each power semiconductor of the CSI requires additional overvoltage protection device (i.e., bi-directional diode) for clamping the commutation voltage transients.

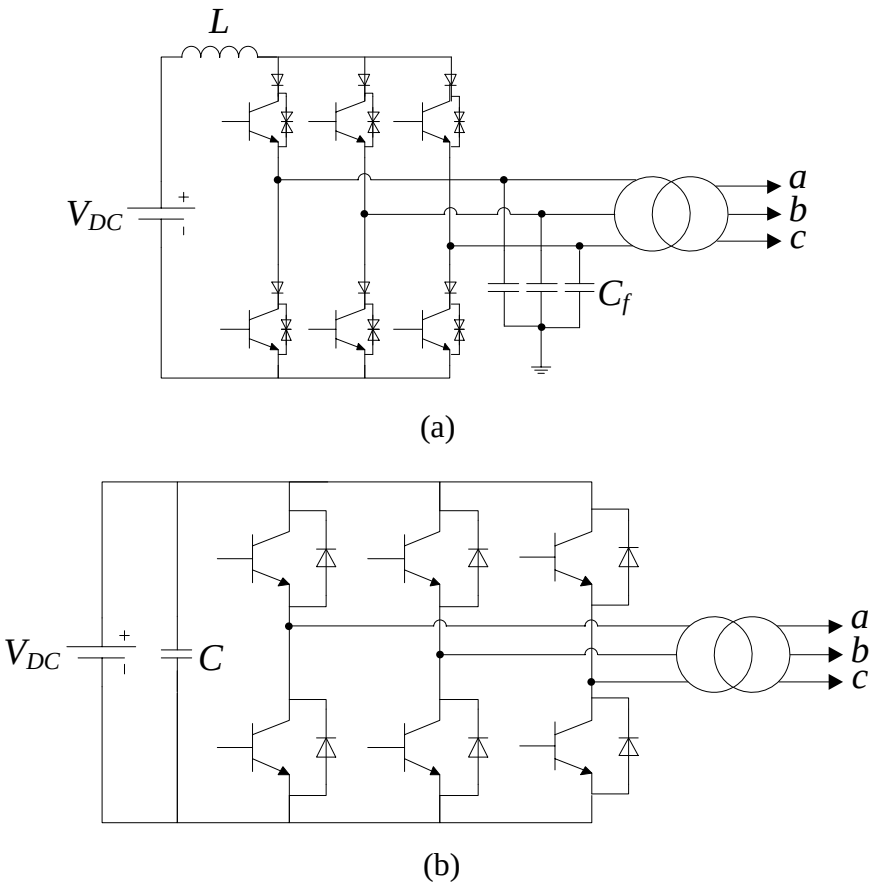


Figure 2-1. Conventional three-phase six-pulse (a) CSI and (b) VSI.

In conclusion, VSI surpasses CSI in terms of construction cost, dynamic performance capabilities, and ease of control. Nevertheless, there are several problems associated with these configurations in high-power applications:

i) Power capability is limited due to the constraint number of series connected power semiconductors;

ii) High PWM switching frequency (i.e., more than 10 kHz) is required to achieve optimal harmonic performance but that comes at the expenses of higher power losses, stress, and heat on the power semiconductors [122]-[124];

iii) Bulky, heavy, and costly line frequency transformer is required to boost the inverter voltage to the grid voltage-level.

These lead to the advent of multilevel inverters as a new type of power inverter option for high-power applications, which can create higher voltages and reduce harmonics by its own circuit topology [25]-[28].

The next subsection discussed different multilevel inverter topologies.

2.2.1.2 Multilevel Inverters

The concept of multilevel VSI was first introduced and patented by Baker and Bannister in 1975 [125]. Since then, plentiful researches and studies have been carried out, aiming to produce a staircase waveform akin to an ideal sinusoidal waveform with better harmonic spectrum. For the last three decades, three main multilevel inverter topologies have been proposed, namely, Multilevel Diode-Clamped Inverter (MDCI), Multilevel Capacitor-Clamped Inverter (MCCI), and MCHI with separated DC sources. Moreover, abundant modulation and control schemes have been developed and implemented for multilevel inverters to cater for different performance requirements.

The following subsections describe the aforementioned multilevel inverter topologies.

2.2.1.2.1 Multilevel Diode-Clamped Inverter

The MDCI topology was unveiled by Nabae in 1981 with a three-level Neutral Point Clamped (NPC) VSI [126]. Consequently, several studies have been reported and published for four- [127]-[128], five- [129]-[134], six- [135]-[139], and eleven-level [136] diode-clamped inverter for various applications including motor drives, Photo-Voltaic (PV), and STATCOM applications. The basic operation principle of MDCI can be found in [27]. As an example, a single-phase five-level diode-clamped inverter is shown in Figure 2-2 with four series capacitors connected across the DC-link.

Generally, an M_N-level diode-clamped inverter requires $2 \times (M_N\text{-}1)$ power semiconductors, $(M_N\text{-}1) \times (M_N\text{-}2)$ clamping diodes, and $(M_N\text{-}1)$ DC-link capacitors.

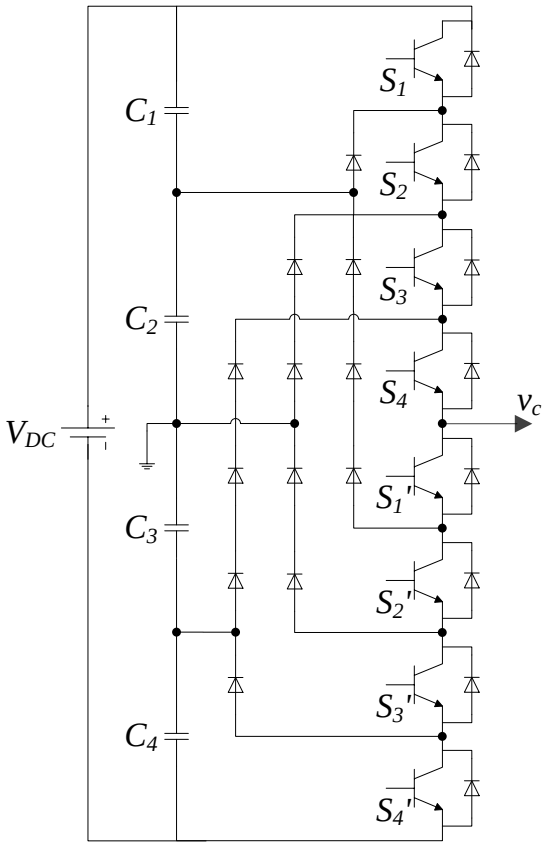


Figure 2-2. Phase-leg of a five-level diode-clamped inverter [140].

These diodes are used to clamp the voltage across each DC capacitor at $V_{DC}/(M_N\text{-}1)$ in order to achieve multi-step output voltage waveform. However, there are a number of drawbacks associated with this topology which are summarized as follows [31], [27]:

i) Different voltage ratings of diodes are required to achieve $V_{DC}/(M_N\text{-}1)$ across each DC capacitor due to unbalance charging and discharging at different levels;

ii) Each inverter level requires different current ratings of power semiconductors due to different duty cycle of operation;

iii) Impractical to implement for an inverter above five-level due to the excessive number of diodes required and DC capacitor voltage balancing issues;

iv) Difficult to get optimized physical power circuit layout due to stray inductance of the interconnection between power components;

therefore, leading to generate overvoltage due to significant rate of current change which may damage the power switches [138].

2.2.1.2.2 Multilevel Capacitor-Clamped Inverter

The MCCI or else known as multilevel flying-capacitor inverter was introduced by Foch and Meynard in 1992 as an alternative topology for the MDCI [141]. This topology uses capacitors instead of diodes to clamp the voltage. In the last decade, several published articles that have reported experimental results for three- [142]-[145], four- [143], and five-level [146]-[151] capacitor-clamped inverters for different applications such as FACTS controllers and variable speed motor drives. Its basic operation principle can be also found in [27]. Figure 2-3 depicts a single-phase five-level capacitor-clamped inverter with four series capacitors connected across the DC-link.

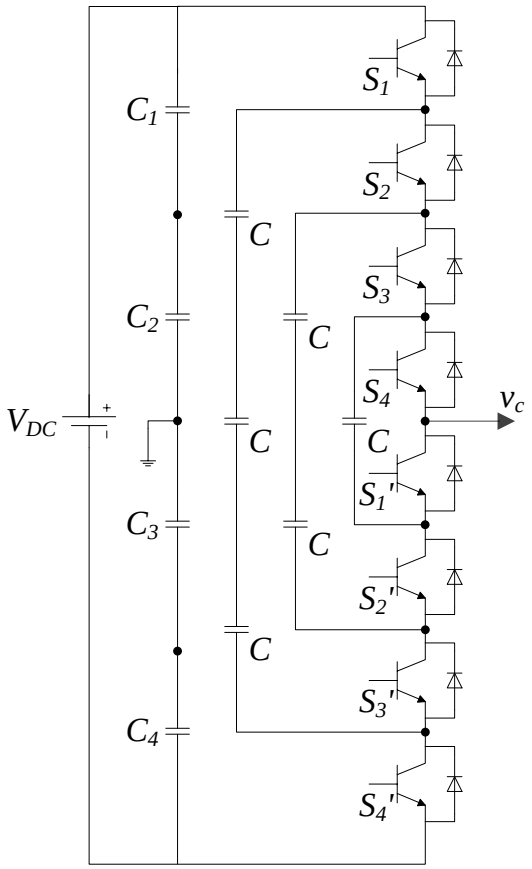


Figure 2-3. Phase-leg of a five-level capacitor-clamped inverter [27].

With similar inverter structure as the MDCI, an M_N-level capacitor-clamped inverter requires a total of $((M_N\text{-}1)\times(M_N\text{-}2))/2$ clamping capacitors

per phase in addition to the M_N-1 main DC-link capacitors. The advantages of the MCCI over the MDCI are summarized as follows:

i) Clamping diodes are not needed;

ii) Large number of capacitors enables better performance during voltage sags;

iii) Phase redundancies are available which can be used to balance the voltage-levels of the flying-capacitors.

However, MCCI also suffers from a number of limitations which are summarized in the following points:

i) Different ratings of power semiconductors are required due to the unequal load distribution among the DC capacitors;

ii) Large number of bulky energy storage capacitors increases the inverter size as the number of levels increases;

iii) Complex control with high-switching frequency is required to balance the voltages across each capacitor [26].

2.2.1.2.3 Multilevel Cascaded H-bridge Inverter

Despite being one of the first multilevel inverter topology to be discovered in 1975, the MCHI was only recognized for its superiority over the past three decades [125]. Several studies have been demonstrated its ability to generate as high as twenty one- [40], [56] and twenty five-level [152] output voltage waveform, which greatly emphasize its many benefits over the formal multilevel topologies in high-power applications [31]-[32]. A single-phase structure of five-level CHI is illustrated in Figure 2-4 as an illustrative example.

As the name implies, this topology connects several H-bridge inverter modules in series to produce the desired staircase output waveform. For instance, an M_N-level CHI requires (M_N-1)/2 H-bridge inverters and (M_N-1)/2 DC sources for each phase-leg to produce M_N-level of output voltage. It is worth noting that the three-phase MCHI can be constructed by connecting

three of these single phases to form either a star or delta configuration [26]. This allows each phase of the inverter to be controlled independently to furnish both positive- and negative- sequence reactive currents.

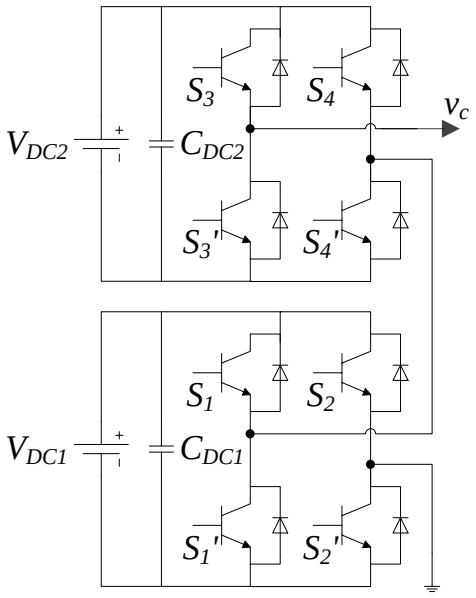


Figure 2-4. Phase-leg of a five-level CHI.

The advantages of the MCHI are summarized in the following points [26]:

i) Simplest architecture with no clamping-diodes and -capacitors required;

ii) All the power semiconductors including the DC capacitors have the same ratings;

iii) Ideal choice for full cell, Hybrid Electric Vehicle (HEV), and photovoltaic applications, where many small DC-power cells are involved.

Nevertheless, MCHI also faces some limitations which are highlighted as follows [27]:

i) Large numbers of isolated voltage source are required to supply each H-bridge inverter;

ii) A failed H-bridge module must be removed or bypassed to avoid short circuit.

2.2.1.3 Comparison among Multilevel Inverters

In power systems application, the motivation behind replacing the conventional VSIs with multilevel inverters is to get rid of the bulky, heavy, and costly line frequency transformer. For instance, it has been reported by Akagi et al. [42] and Jimichi et al. [153] that the weight of a three-phase frequency transformer rated at 6.6 kV and 1 MVA ranges from 3000 to 4000 kg, while the weight of the three-phase MCHI with the same voltage and current ratings may ranges from 1000 to 2000 kg. Moreover, [154] has also shown that the transformer weights about half of the 360 kVA D-STATCOM system. Additionally, these transformers represent about 70% from the total power losses of the MVA rating of the STATCOM system [155].

Obviously, the superiority of a multilevel inverter is proportional to the number of levels. As the level increases, low harmonic sinusoidal voltage waveforms can be achieved with low-switching frequency PWM technique. However, the number of voltage-levels as well as the system reliability is limited by the control complexity, complication of the system structure, and cost-ineffectiveness. Table 2-1 illustrates the total number of components needed for the aforementioned multilevel inverters to achieve the same number of voltage-levels, M_N.

Table 2-1. Comparison of total component requirements per phase-leg among three multilevel inverter topologies.

Multilevel inverter Topology	**MDCI**	**MCCI**	**MCHI**
Power semiconductor switch with anti-parallel diode	$2\times(M_N\text{-}1)$	$2\times(M_N\text{-}1)$	$2\times(M_N\text{-}1)$
Clamping-diode	$(M_N\text{-}1)\times(M_N\text{-}2)$	0	0
Clamping-capacitor	0	$((M_N\text{-}1)\times (M_N\text{-}2))/2$	0
DC-link Capacitor	$M_N\text{-}1$	$M_N\text{-}1$	$(M_N\text{-}1)/2$
Total	$\boldsymbol{M_N^2\text{-}1}$	$\boldsymbol{(M_N^2+3\,M_N\text{-}4)/2}$	$\boldsymbol{(5\,M_N\text{-}5)/2}$

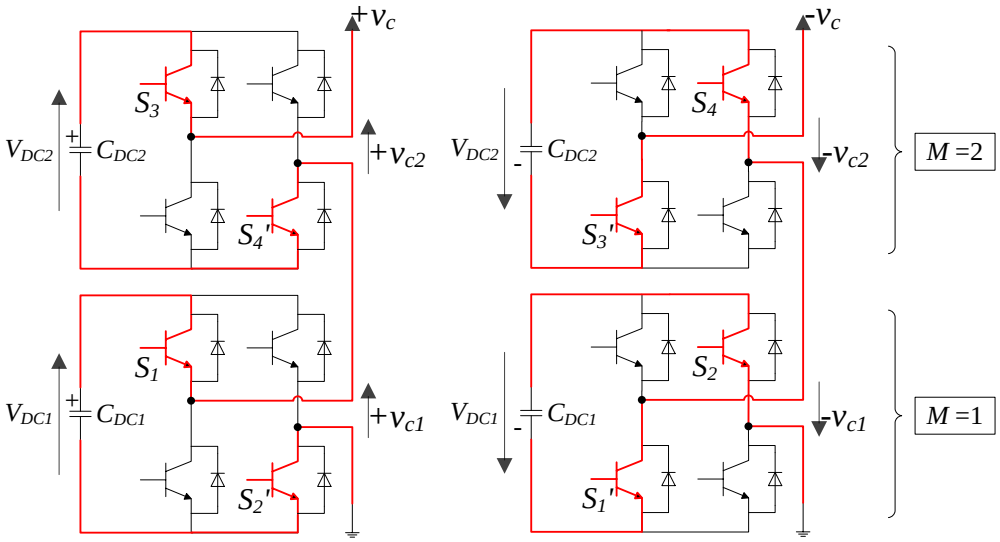
From Table 2-1, the MCHI topology requires the least number of components to synthesize the same voltage-levels. Because it does not require any clamping-diodes or -capacitors, the circuit layout can be fully maximized and packaging is made easy due to its repetitive structure. In addition, the MCHI topology can be easily adapted to ESS applications (i.e., fuel cell, PV cell, ultra-capacitor bank, etc.), enabling real current compensation capability in a STATCOM system.

Furthermore, the size of the DC capacitor has an impact on the cost and size of the FACTS controller. For instance, a method for dimensioning the DC capacitor was presented by Soto et al. [156] for four inverter topologies (i.e., one multipulse and three multilevel: MDCI, MCCI, and MCHI). The work shows that for balanced operation (i.e., positive sequence current), the multipulse topology requires the lowest DC capacitor rating followed by the MDCI and MCHI topologies. However, if the inverter must support significant negative sequence current, then the capacitance rating of the multipulse, MDCI, and MCHI topologies become similar. The work also shows that the MCCI topology has the highest capacitor rating under all circumstances. Nevertheless, it was concluded that given a requirement for negative sequence current, the MCHI topology is still an attractive implementation for a STATCOM amongst the inverters examined.

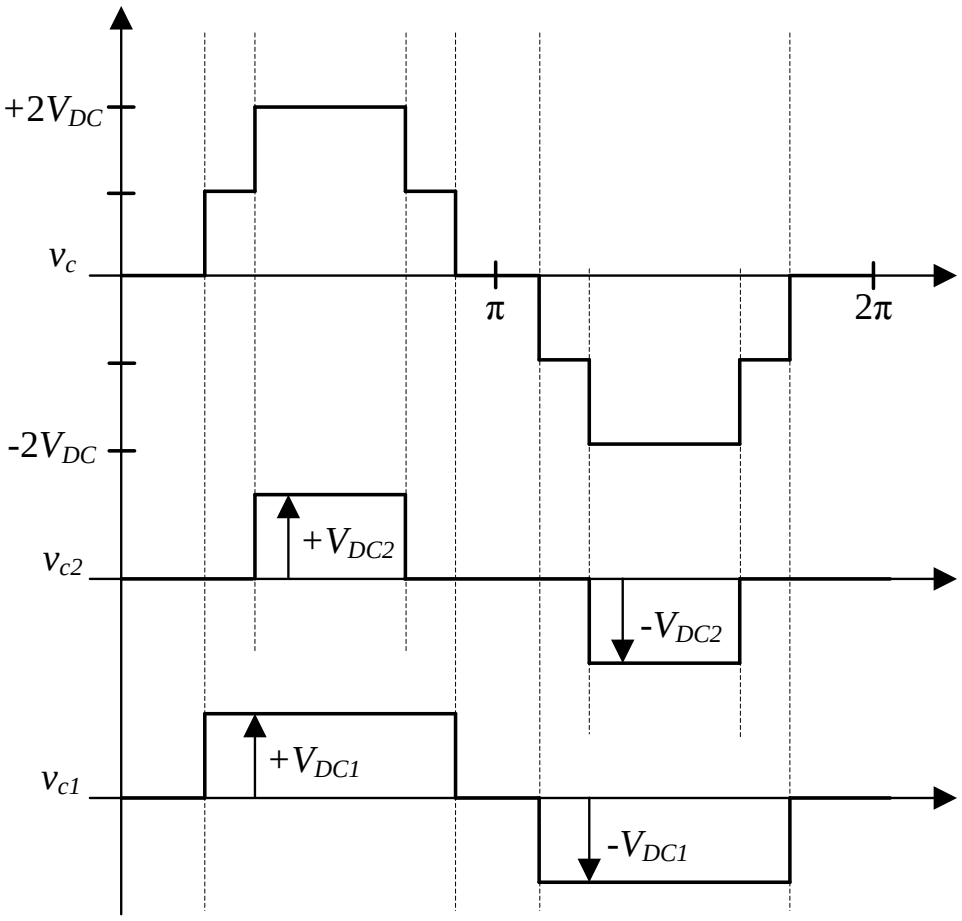
The operating principle of the MCHI is briefly discussed in the next subsection.

2.2.1.4 Operating Principle of Multilevel Cascaded H-Bridge Inverter

A single-phase five-level CHI and its functional operation to generate one complete cycle of a sine wave is illustrated in Figure 2-5. The MCHI phase voltages v_c are synthesized by summing of equal DC-levels (i.e., $+V_{DC}$, 0, $-V_{DC}$) from each H-bridge cell. Each leg of an H-bridge inverter which is formed by two series-connected switching devices, should switch-on complementary to avoid short-circuiting across the DC-link. This can be achieved by appropriate a dead-band time between each switching device to ensure that either one of them is completely off before switching-on the other one.



(a) (b)



(c)

Figure 2-5. Operation of five-level CHI to generate (a) positive half-cycle, (b) negative half-cycle, and (c) the associated AC voltage waveform.

As with other VSI topologies, a control strategy is required to regulate the DC voltage-levels of each cell in order to produce a high-quality output waveform. Several voltage balancing methods have been proposed particularly for the MCHI. Some researches proposed a control algorithm based on clustered and individual cell voltage balancing methods consisting of closed loop feedback PI-controllers [32], [42]. Another proposed a switching pattern swapping scheme (see Figure 2-6) to resolve the imbalance device stress and achieve voltage balance control [33].

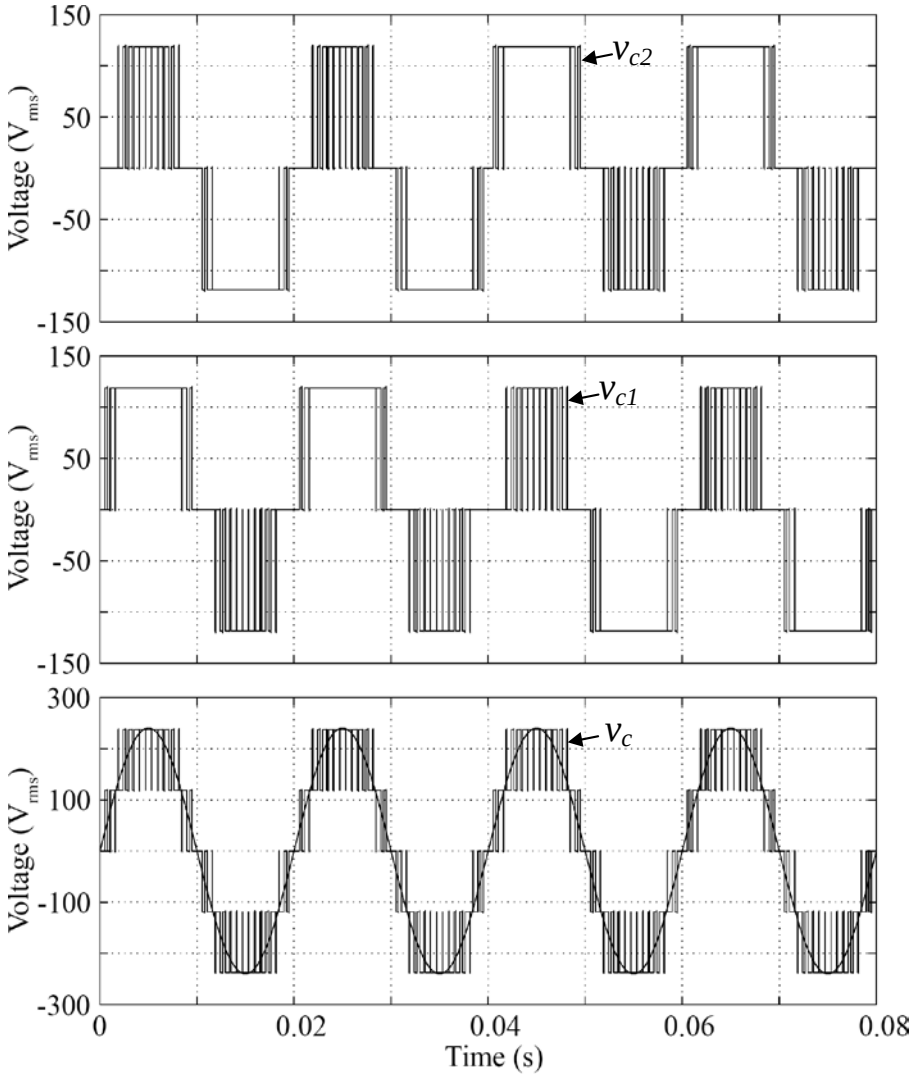


Figure 2-6. Five-level voltage waveforms generated via CB-PWM technique with switching pattern swapping scheme.

All these experimental validations of balancing methods are simulated for STATCOM applications and results indicated that the STATCOM is capable

of providing satisfactory compensation with balanced DC-link regulation. Apparently, the MCHI topology offers the most simple and reliable voltage balancing methods compared with other multilevel inverters [25]-[28].

2.2.2 STATCOM Modulation Techniques and Control Schemes

Contemporary research on MCHI has produced unique modulation techniques and novel control schemes which are generally classified into two categories in relation to the switching frequency. Representatives of techniques operate with fundamental or low-switching frequencies are the SVM and MSHE-PWM. These modulation techniques can perform one or two commutations of the power semiconductors to generate one cycle of staircase voltage waveform. On the other hand, CB-PWM technique operating with high-switching frequency performs many commutations of the power semiconductors in one cycle to generate a fundamental output voltage.

The following subsections briefly report the most commonly employed modulation techniques for MCHI.

2.2.2.1 Carrier Based Pulse Width Modulation

CB-PWM is by far the simplest technique to generate multilevel pulse trains through the intersection of a fundamental reference waveform with the preferred disposition carriers. There are three well-known disposition methods, namely:

i) In-Phase Disposition (IPD) (see Figure 2-7(a)): All carriers are in phase;

ii) Alternative Phase Opposite Disposition (APOD) (see Figure 2-7(b)): Each carrier is phase shifted by 180º from its adjacent carrier;

iii) Phase Opposite Disposition (POD) (see Figure 2-7(c)): All carriers above zero reference point are 180º out-of-phases with those below the zero reference point.

A comparative evaluations of these methods based on THD performance for multilevel inverter topologies with respect to the number of levels, switching

frequencies, and modulation indices have been reported in several articles [62]-[63]. Specifically, Agelidis and Calais [62] reported that the IPD has better THD and distortion factors in both the linear and over-modulation regions when compared with the APOD and POD methods.

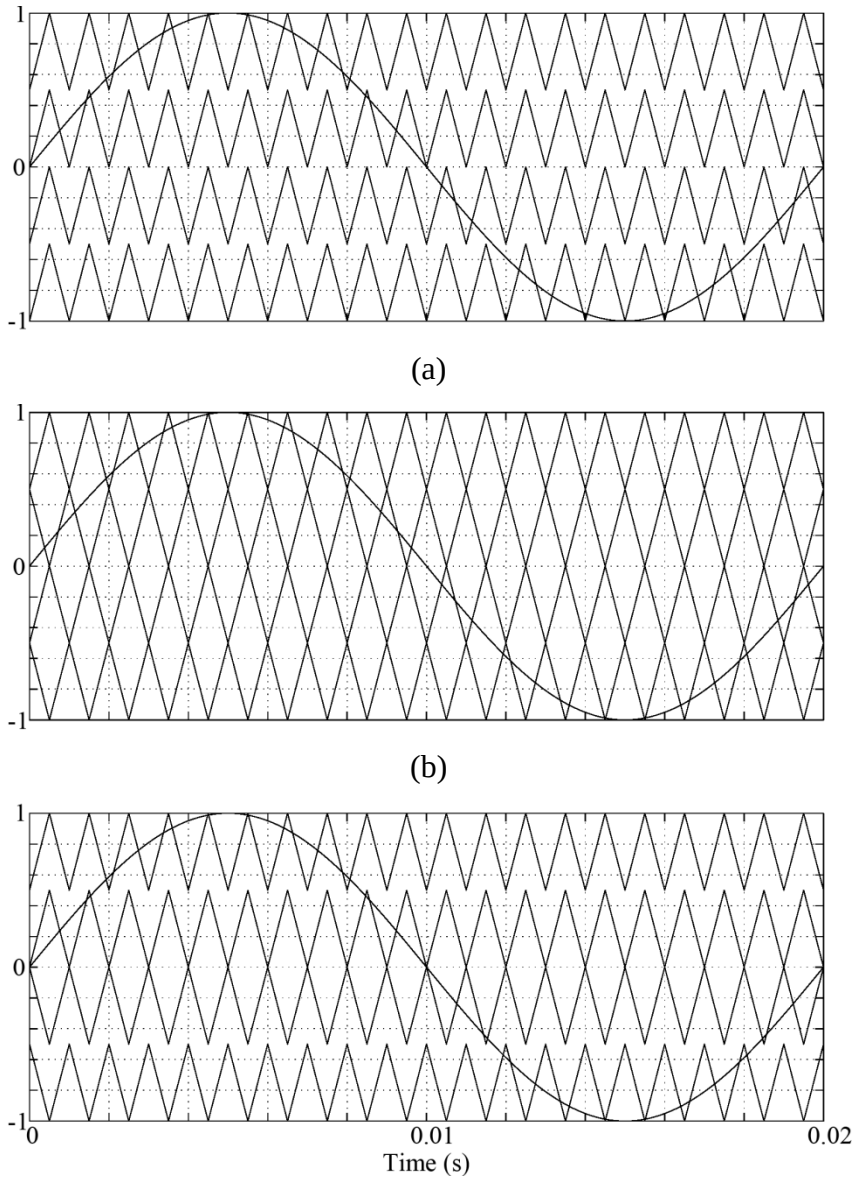


Figure 2-7. CB-PWM technique for single-phase five-level inverter with (a) IPD, (b) APOD, and (c) POD method.

McGrath and Holmes [63] also showed that the IPD favorably offers the best harmonic performance for multilevel inverters. Zero sequence injected IPD CB-PWM or else known as the Switch Frequency Optimal (SFO) PWM technique, with marginal THD improvement was presented by Wu and He [64]

and later by Tolbert et al. [65] and Yao et al. [66] to further enhances the THD performance in lower modulation indices with additional switching instants.

Despite its simplicity, the CB-PWM technique does not offer any direct manipulation over the harmonic contents and yet exhibits high-switching losses due to high-switching frequencies; restricting its application in high-power systems where high-losses are intolerable [67]. Furthermore, in this switching scheme, the maximum MI for linear operation is 1.0 and the fundamental component will not increase linearly in the over-modulation range.

2.2.2.2 Space Vector Modulation

SVM technique can alternatively be used to manipulate harmonics at low-modulation indices and maintain desired performance characteristics of multilevel inverter in low-switching frequencies [66]-[69]. It was first presented by Kovacs and Racz [70] in 1959 and subsequently in 1980s by Pfaff et al. [71] and van der Broeck [72] based on the concept of a rotating space vector representation of the voltages in the *dq* plane (see Figure 2-8).

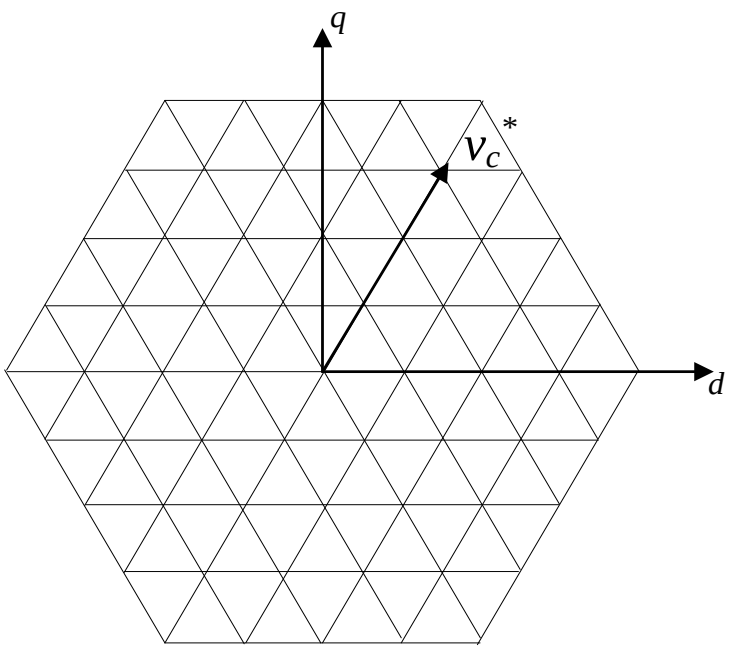


Figure 2-8. SVM diagram for single-phase five-level inverter.

When compared with CB-PWM technique, the SVM has additional features such as good utilization of DC-link voltage, low-current ripple, and relatively

easy hardware implementation using DSP boards. These features make it suitable for high-voltage high-power applications [27]. For the last decade, efforts have been made to extend the operation of multilevel inverters under SVM in the over-modulation region [73]-[77]. However, as the number of levels increases, the number of switching states also increases drastically, resulting in difficulty to compute the duty cycles, selection of the proper switching states, and determination of sectors in which the reference vector lies in. Further efforts to eradicate these problems have been attempted to simplify the computation and control [78]-[79]. However, as the number of level decreases, the error in terms of the generated vectors with respect to the reference will be higher and hence, causing an increase in current ripple that affects the capacitor lifetime [152].

2.2.2.3 Multilevel Selective Harmonic Elimination Pulse Width Modulation

MSHE-PWM, on the other hand, is a pre-programmed PWM method that offers a tight control of the low-order harmonics with considerable low-equivalent switching frequency when compared with the formal modulation techniques; therefore, leading to low-switching power loss (i.e., 40% of reduction [80]) and good harmonic performance.

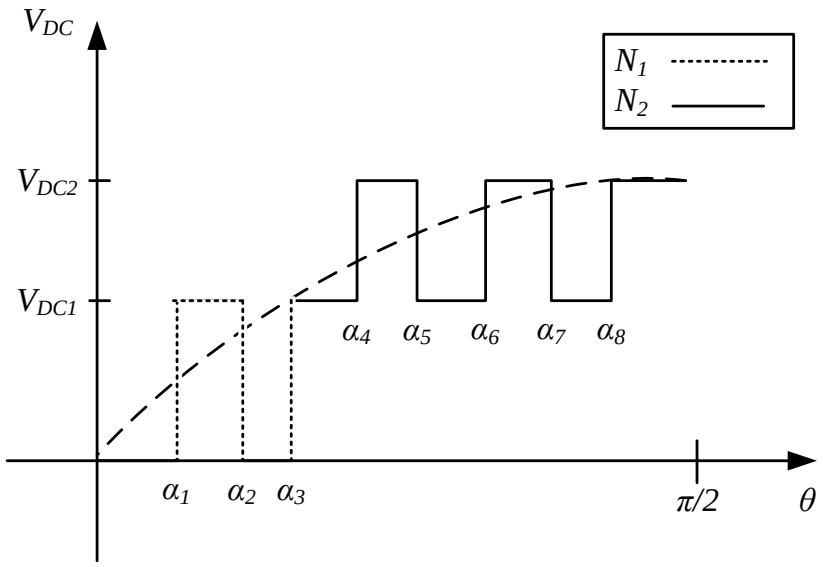


Figure 2-9. Single-phase five-level SHE-PWM waveform (only quarter-cycle shown).

Thus, this technique is considered a competitive solution for medium- and high-power conversion systems such as STATCOM and other utility based inverters. The in-depth review of MSHE-PWM technique covering the most recently developed and published methods can be found in several articles of the literature such as [80].

This carrier-less technique was proposed by Patel and Holf [81] in 1973, which used Fourier series to analyse and express the harmonic contents mathematically by a group of non-linear and transcendental equations. For instance, the Fourier series that represents the odd quarter-wave symmetry of voltage V_{DC} waveform (see Figure 2-9) with period $L = \pi/2$ is given as follows:

$$V_{DC}(t) = a_0 + \sum_{n=1}^{\infty}\left[a_n \cos\frac{n\pi t}{L} + b_n \sin\frac{n\pi t}{L}\right] \tag{2-1}$$

where each coefficient formula is defined by:

$$a_0 = \frac{1}{2L}\int_{-L}^{L} V_{DC}(t)dt \tag{2-2}$$

$$a_n = \frac{1}{L}\int_{-L}^{L} V_{DC}(t)\cos\left(\frac{n\pi t}{L}\right)dt \tag{2-3}$$

$$b_n = \frac{1}{L}\int_{-L}^{L} V_{DC}(t)\sin\left(\frac{n\pi t}{L}\right)dt \tag{2-4}$$

Since V_{DC} is assumed to be an odd function (i.e., $V_{DC}(t) = -V_{DC}(-t)$), hence, the integral of (2-2) can be written in the following way:

$$\begin{aligned} a_0 &= \frac{1}{2\left(\frac{\pi}{2}\right)}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} V_{DC}(t)\,dt = \frac{1}{\pi}\left(\int_{-\frac{\pi}{2}}^{0} -V_{DC}(-t)\,dt + \int_{0}^{\frac{\pi}{2}} V_{DC}(t)\,dt\right) \\ &= \frac{1}{\pi}\left(\int_{0}^{\frac{\pi}{2}} -V_{DC}(t)\,dt + \int_{0}^{\frac{\pi}{2}} V_{DC}(t)\,dt\right) = 0 \end{aligned} \tag{2-5}$$

Same approach is applied to (2-3), where the even function (i.e., $\cos(t) = \cos(-t)$) times the odd function (i.e., $V_{DC}(t) = -V_{DC}(-t)$) is odd. This yield:

$$
\begin{aligned}
a_n &= \frac{1}{\frac{\pi}{2}} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} V_{DC}(t) \cos\left(\frac{n\pi t}{\frac{\pi}{2}}\right) dt \\
&= \frac{2}{\pi}\left(\int_{-\frac{\pi}{2}}^{0} -V_{DC}(-t)\cos(-2nt)\,dt + \int_{0}^{\frac{\pi}{2}} V_{DC}(t)\cos(2nt)\,dt \right) \\
&= \frac{2}{\pi}\left(\int_{0}^{\frac{\pi}{2}} -V_{DC}(t)\cos(2nt)\,dt + \int_{0}^{\frac{\pi}{2}} V_{DC}(t)\cos(2nt)\,dt \right) \\
&= \frac{2V_{DC}}{\pi}\left[-\frac{\sin(2nt)}{2n} + \frac{\sin(2nt)}{2n} \right]_{0}^{\frac{\pi}{2}} = 0, \text{for all } n
\end{aligned}
\tag{2-6}
$$

On the other hand, the product of two odd functions (i.e., $\sin(t) = -\sin(-t)$ and $V_{DC}(t) = -V_{DC}(-t)$) is even. Hence, the integral of (2-4) is written in the following way:

$$
\begin{aligned}
b_n &= \frac{1}{\frac{\pi}{2}} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} V_{DC}(t) \sin\left(\frac{n\pi t}{\frac{\pi}{2}}\right) dt \\
&= \frac{2}{\pi}\left(\int_{-\frac{\pi}{2}}^{0} \left[-V_{DC}(-t)\right]\left[-\sin(-2nt)\right] dt + \int_{0}^{\frac{\pi}{2}} V_{DC}(t)\sin(2nt)\,dt \right) \\
&= \frac{2}{\pi}\left(\int_{0}^{\frac{\pi}{2}} V_{DC}(t)\sin(2nt)\,dt + \int_{0}^{\frac{\pi}{2}} V_{DC}(t)\sin(2nt)\,dt \right) \\
&= \frac{4}{\pi}\left(\int_{0}^{\frac{\pi}{2}} V_{DC}(t)\sin(2nt)\,dt \right) = \frac{4V_{DC}}{\pi}\left[-\frac{1}{2n}\cos(2nt) \right]_{0}^{\frac{\pi}{2}} \\
&= \frac{4V_{DC}}{\pi}\left(-\frac{1}{2n}\cos\left(2n\left(\frac{\pi}{2}\right)\right) - -\frac{1}{2n}\cos(0) \right) \\
&= \frac{2V_{DC}}{n\pi}\left(-\cos(n\pi)+1\right) = 0 \qquad , n \text{ is even} \\
&= \frac{4V_{DC}}{n\pi} \, , n \text{ is odd.}
\end{aligned}
\tag{2-7}
$$

Based on (2-5)-(2-7), the Fourier series of (2-1) is reduced to:

$$
V_{DC} = \sum_{n=1,3,5\ldots}^{\infty} \left[b_n \sin(n\alpha) \right] \tag{2-8}
$$

where $\alpha = \pi t / L$.

By referring to (2-7)-(2-8) and Figure 2-9, a generalised expression of b_n for five-level SHE-PWM waveform with eight number of switching angles (i.e., $N_1 + N_2 = 8$) and is given by:

$$b_n = \frac{4}{n\pi}\left(V_{DC_1}\sum_{\iota=1}^{N_1}(-1)^{\iota+1}\cos(n\alpha_\iota) + V_{DC_2}\sum_{\iota=N_1+1}^{N_1+N_2}(-1)^{\iota}\cos(n\alpha_\iota)\right) \tag{2-9}$$

where N_1 is the odd number of switching transitions between zero- and the first-level, N_2 is the number of switching transitions between the first-level and the second-level which can be either odd or even number, and α_i is the i^{th} switching angle.

By equating the first harmonic component (i.e., n = 1) to the desired voltage and then equating all the unwanted harmonics (i.e., n = 3, 5, 7, and etc.) to zero, multiple solutions of switching angles can be computed offline by using programmed mathematical methods (i.e., Newton-Raphson [82], neural networks [83], Walsh functions [84], genetic algorithm [85], resultant theory [86], homotopy algorithm [87], and etc.). These solutions are usually stored in the memory look-up tables for real-time system implementation so that the performance will not be limited by the power of DSPs. However, the drawback of this technique is that the computational time becomes more complicated as the number of the intended harmonics to be eliminated increased and in many cases, the solution is not obtainable; therefore, the number of harmonics to be eliminated is usually kept relatively low.

For the last two decades, MSHE-PWM methods have been studied for multilevel inverters and a number of approaches have been reported in the literature for different design objectives. For instance, a generalized formulation for SHE-PWM control dedicated to high-voltage high-power MCHI with both equal and non-equal DC sources that normally employed in constant frequency utility applications was addressed by Dahidah and Agelidis [93]. Another generalized formulation of quarter-wave symmetrical SHE problems was presented by Fei et al. [94]. Other approaches have also been reported, where the SHE-PWM waveforms defined by the well-known carrier-based PWM were proposed by Agelidis et al. [91] as well as Dahidah and

Agelidis [92]. Particle Swarm Optimization (PSO) technique was also introduced as a method for optimizing the cost functions in order to provide solutions to the multilevel SHE problem, where a minimization of the THD rather than a complete elimination of low-order harmonics was the target for both equal [95] and non-equal DC sources [96]. On the other hand, the limitation of quarter-wave symmetrical waveform has been abolished while half-wave [97] and non-symmetrical waveforms [88] have also been analysed. A novel systematic design approach applying signal processing methods to modify adaptive SHE algorithms was reported by Blasko [89]. Watson et al. [90] presented a complete harmonic elimination method that balances DC-link voltages in a multilevel cascaded H-bridge rectifier. A new formulation of SHE-PWM technique suitable for MCHI was recently reported by Dahidah et al. [98] and Law et al. [99], where the DC voltage-levels were made variant to increase the degree of freedoms in the formulation of MSHE-PWM and hence, the number of harmonics to be eliminated (i.e., (N+M)-1 as opposed to N-1) without changing the physical structure of the inverter. The technique also eases the online implementation for dynamic systems.

The following subsection reports the most commonly employed control schemes for MCHI.

2.2.2.4 VAR/Harmonic Compensation Control Scheme

In order to compensate for VAR and/or harmonics, different control schemes based on frequency- or time-domain technique have been developed to compute the reference currents which needed to be drawn or injected to/from the PCC. Furthermore, the time-domain technique is much preferred than its counterpart due to its practicality as well as the ability to compute the reference currents and track load changes almost instantaneously [156]. For the past three decades, two well-known time-domain strategies, namely, the *pq*- and *dq*-method, have been proposed to specify the performance of a STATCOM system. Particularly, the *pq*-method, at first, used Clarke's transformation to convert the three measured vectors into $\alpha\beta$ stationary reference frame yielding instantaneous active p and reactive q power components [158] (see Figure 2-10). In general case, each of the active

and reactive powers are composed of continuous (i.e., fundamentals) and alternating (i.e., harmonic components) terms. A low-pass filter with feed-forward structure [159] or fifth-order 50 Hz cut-off frequency [160] can be used to separate the continuous and alternating terms of the active and reactive instantaneous power.

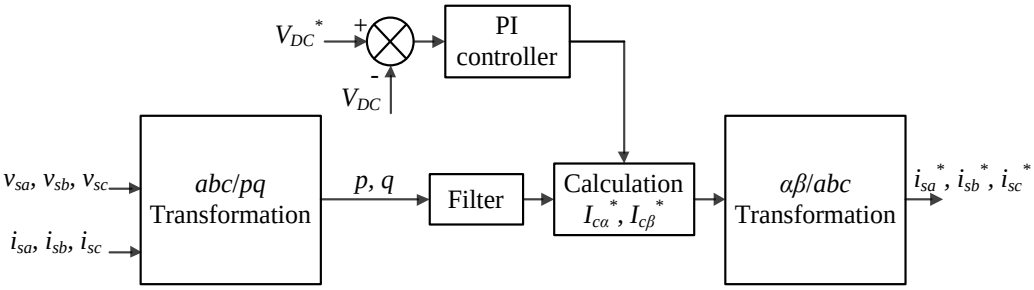


Figure 2-10. STATCOM control block diagram using *pq*-method.

When compared with the *dq*-method, *pq*-method offers much simpler control scheme as it requires less transformation [160]. However, the algorithm fails to capture any harmonic components and reproduce sinusoidal grid reference current when the grid voltages are unbalanced [161]. Moreover, the control computations must involve the zero-sequence term in order to perform load balancing. A study suggested a new time-domain algorithm which provides flexible control and fast transient response (i.e., 6 cycles) to compensate the VAR and/or harmonics in distorted single-phase power system [162]. Another algorithm based on the power Fryze's theory was reported by Petit et al. [163] to deal with three-phase systems under non-sinusoidal voltage situations. Li et al. [164] presented a novel current-detection algorithm based on time domain for determining the compensating current reference. The algorithm proved to be simpler, faster response (i.e., 2 cycles), and more accurate when compared with the analogue method (i.e., derived components has magnitude and phase errors) [165], the instantaneous reactive power theory method (i.e., unable to detect the selective order harmonics) [166], and the Fourier transform based method (i.e., unable to split the fundamental component into the positive- and negative-sequence component) [167]. Nevertheless, these algorithms require a large amount of calculation due to complexity and thus, making the control circuits hard to be implemented. An interesting assessment of the current

reference computation error (i.e., based on the THD of grid current) as a function of load voltage distortion for the *dq*- and *pq*- method was demonstrated by Ortega et al. [168]. It was concluded that the *dq*-method showed the largest error in the negative-sequence of the 5th harmonic, whereas the *pq*-method showed the highest positive-sequence of grid current THD value.

The *dq*-method, on the other hand, uses both the Clarke- and Park-transformations to convert the three measured vectors to *dq* components [169] (see Figure 2-11). From Figure 2-11, the *abc*-to-*dq* transformation or else known as SRF requires phase angle synchronization which can be easily achieved using Phase-Locked Loop (PLL) circuits. Each direct *dq* component is filtered off using suitable filtering circuit when computing the reference current for total compensations (i.e., VAR/harmonics/unbalance). Because all the computations involved are in DC quantities, the control system proves to be very stable even with unbalanced systems. However, the computations might incur some time delays due to the filtering of the DC quantities, and the algorithm is also fairly complicated because it involves various transformations.

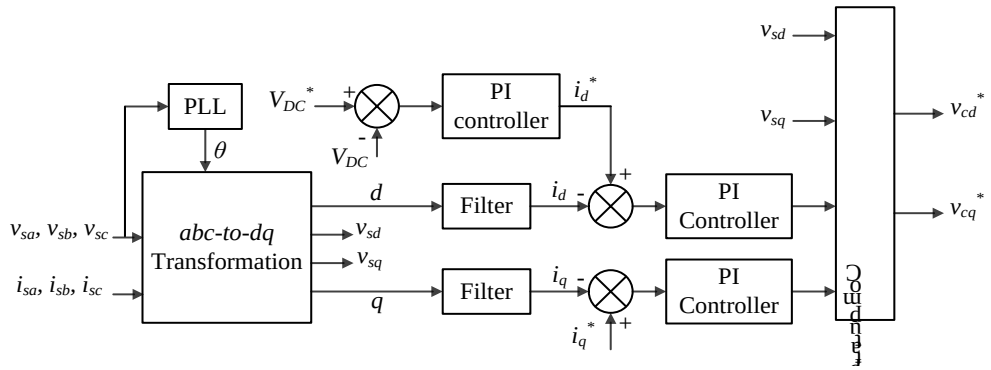


Figure 2-11. STATCOM control block diagram using *dq*-method.

In other words, the compensation precision substantially relies on the ability of the PLL to track the phase angles as well as the filter design. Nevertheless, the *dq*-method, which incorporates decoupling feed-forward/feedback systems with appropriate control algorithms, is commonly used to achieve lower steady-state errors and acceptable transient characteristics in response to a step change of the loading conditions [29].

For instance, an eleven-level CHI based STATCOM was demonstrated by Peng et al. [31] using the *pq*-method then later by Peng and Lai [32] and Peng et al. [33] with the *dq*-method to further enhance the dynamic performance and achieve DC voltage balance control for VAR compensation, respectively. However, the formulation to obtain each gain of the PI-controller used for the active and reactive current loops is not provided.

Liang and Nwankpa [34] presented a formulation to reject the STATCOM current harmonic component caused by the DC capacitor voltage ripple along with the criteria for sizing the DC capacitor. The work shows that faster dynamics is achieved by employing the MI regulation method in STATCOM system. Additionally, the STATCOM output voltage waveform dropped one-level (i.e., from seven- to five-level) during inductive mode of operation to achieve lower fundamental component value.

A five-level CHI based STATCOM system incorporating ESS was proposed by Qian and Crow [35] to achieve power oscillation damping, active power flow control, and four quadrants operation. However, poor dynamic and transient responses are attained by the use of decoupled PI control scheme as it took approximately 50 cycles to detect and restore the grid voltage back to a unity and then reached steady-state.

In [37], an Automatic Gain Controller (AGC) was proposed to reduce the influence of the high grid impedance and mitigate the effect of the inherent PLL delay, which is the source of oscillations exhibited by the STATCOM under different loading conditions. The method was further utilized by Sundaraju and Kumar [53] to reduce the effect of the PLL delay. However, overshoots in STATCOM current (i.e., three times higher than the rated current) still occur during the changes in loading condition, causing the need of higher rating power components as well as threatening the system stability due to poor transient response (i.e., 15 cycles to reach steady-state) [38].

A selective harmonic control based passivity theory incorporated with P-controller was presented by Escobar et al. [9] to achieve VAR, unbalance, and harmonic compensations under distorted and unbalanced operating conditions. Although the control loop consists of second-order low-pass filters to reduce the effects of signal distortion, the controller still enables fast tracking of the command values (i.e., 5 cycles to reach steady-state) and

compensation of delay inherent to the digital implementation. However, this was accomplished with high-switching frequency (i.e., 10 kHz) to attain the desired current loop bandwidth. Moreover, when it was compared with PI-controller, the distortion of residual grid current due to the 5^{th}, 7^{th}, and 13^{th} harmonics generated by the load is only marginally reduced.

A modified "*i*cos*φ*" control algorithm which is based on the extraction of the fundamental load current and grid voltage using second-order low-pass filter, was applied to a three-level inverter [39]. However, the delays caused by these filters limit the bandwidth of the regulator control loops; hence, deteriorating the dynamic performance of the controller. This has been further confirmed by [40], where the authors claimed that transient performance of an inverter is determined by the delay around the control loop and the switching frequency of the inverter.

In [41], an experimental work from a scaled down prototype was developed to present a time-domain control scheme with its proposed modulation technique in order to prevent the inverter's transformer from DC magnetization problem. However, it was concluded that the PI-controller may not be robust enough due to the variations of parameters and operating points, which may block the STATCOM due to the overcurrent caused by the dynamic overshoot.

The clustered and individual balancing controls were proposed by Akagi et al. [42] to balance the voltage of multiple separated DC capacitors without restriction on the cascaded number. However, the proposed control scheme involves two extra PI-controllers for each phase-leg, resulting difficulty to assign appropriate values to the gain parameters for realizing the cascade PWM STATCOM with various voltage and current ratings.

Another control scheme with fixed MI and variable DC capacitor voltage-levels was presented by Chen and Hsu [43] to provide VAR compensation and voltage regulation. When MI was fixed for both capacitive and inductive operating modes, low-THD is achieved without utilizing a harmonic elimination technique and with a switching frequency of about 2 kHz. However, this led to poor dynamic performance, where it took approximately 10 fundamental cycles to restore the grid voltage back to a unity and then reached steady-state.

Song and Liu [44] proposed a control scheme to simultaneously achieve reference current tracking and DC-link voltage balancing under unbalanced conditions. However, since low-pass filters were used to separate the positive- and negative-sequence components of the load currents; therefore, the settling time of the reference current determination block cause voltage and current transients when the unbalance occurred.

In [45], the authors claimed that a traditional PI-controller with constant parameters may not be robust enough due to the variations of system parameters. Thus, a fuzzy-PI-based direct-output-voltage control scheme with immunity capability of uncertainties in the STATCOM system was introduced to simultaneously regulate the voltages at the PCC as well as DC-link voltage; forcing the system to return back to steady-state value faster than the PI-controller. However, the design process of fuzzy control involves defining complicated rules and factors that relate the input variables to the output model properties while offering only moderate improvement of compensating performance over the conventional PI-controllers.

A self-tuning PI-controller using PSO algorithm was extended to the STATCOM aiming to achieve satisfactory dynamic response under balanced load [46]. When compared with the formal fuzzy approach, the PSO method does not require inference rules to obtain the controller gains, instead, it requires an evaluation function, which attained by the Runge-Kutta numerical method to specify the performance of the control system in real-time applications. Nevertheless, these two approaches (i.e., fuzzy and PSO) involve complex formulations which increase the computational burden of digital signal processor.

An integrated control which incorporates both the voltage and current controls to compensate the unbalance problem caused by the load and the grid voltage was proposed by Xu et al. [47]. Nevertheless, the work reported that with no ESS integrated into the STATCOM system, the degree of unbalance to be compensated is low.

In [48], PI-controllers were considered to provide voltage and current regulations for STATCOM based on nine-level CHI. Although good dynamic response was achieved, yet a variation of reactive current i_{cq} which leads to

poor transient response and hence, instability of the proposed system still can be obviously seen in steady-state operation.

Yazdani et al. [49] proposed an approach to reconfigure an eleven-level CHI based STATCOM during a switch failure, along with an interesting comparison between the fault detection methods, namely, the voltage frequency analysis, Artificial Intelligence (AI) based fault detection, and the proposed method.

A hybrid PWM scheme was reported by Wang et Al. [50] to achieve good THD performances during the steady-state operation (i.e., provided by SHE-PWM technique with low-switching frequency) and effective suppression of the transient resonance during a load step change (i.e., attained by SVM technique with high switching frequency), respectively. However, the transition between the two modulation techniques during a load step change led to large peak transient oscillations and resonances in the AC waveforms that could damage the switching devices.

An interesting comparison between three types of balance control scheme, namely, the active voltage vector superposition, MI regulation, and phase shift angle regulation has been reported by Liu et al. [52] for delta-connected twelve-level CHI topology controlled by CB-PWM technique. It was concluded that the former offers good control performance with strong regulation capability followed by the phase shift angle regulation method and MI regulation method.

A Model Predictive Control (MPC) scheme was reported by Townsend et al. [54] for a nineteen-level CHI based STATCOM to simultaneously balance the DC-link capacitor voltages, minimize the inverter switching losses, and provide good current reference tracking. This scheme was further improved by Townsend et al. [58] by incorporating SVM technique to reduce the switching losses and DC capacitor voltage ripple.

Hagiwara et al. [55] proposed a control method that utilizes the circulating current flowing inside the delta-connected windings to achieve negative-sequence reactive current control. However, high-switching frequency (i.e., 12 kHz) was selected to achieve good performance by overcoming the delay caused by the extraction of the required fundamental components.

A new Modified Selective Swapping (MSS) algorithm was presented by Gultekin et al. [56] as well as Gultekin and Ermis [59] along with the design and implementation of twenty one-level CHI based STATCOM to provide VAR compensation. The method was compared with the conventional swapping scheme to balance the DC-link capacitor voltages and it was concluded that the MSS outperforms the latter in terms of DC-link voltage ripple but at the expenses of higher switching frequency and hence, switching losses.

Another reactive current compensator based direct current control method using triangle carrier wave was proposed by Li et al. [57]. Despite to the precise and fast tracking current performance achieved by this method, an oscillation of the measured STATCOM current was still observed, which can potentially cause voltage instability in weak power systems.

2.3 Summary

This chapter has presented the principle operation and configuration of STATCOM, covering all four-quadrant of operation and different voltage source inverters topologies along with their modulation techniques and control schemes. The investigation started with the conventional (i.e., two-level) inverters in three-phase configurations following by the different multilevel inverter topologies, namely, diode-clamped, capacitor-clamped, and cascaded H-bridge multilevel inverters that were concisely viewed in the light of their performances and use in different applications. The MCHI is especially advantageous in high power applications due to its modular structure and ease of control with a higher number of levels.

Next, various modulation techniques, namely, CB-PWM, SVM, and MSHE-PWM suitable for MCHI reported were presented and studied. MSHE-PWM provides a possible method for reducing the switching frequency without compromising the low frequency harmonic content of the waveform.

Finally, a particular attention has been paid to the control schemes since it is the subject of this research. Numerous methods that have been developed and widely employed to MCHI based STATCOM were reported in the light of their advantages and/or disadvantages in order to strengthen the

background of this dissertation and also to justify the contributions of the proposed work.

The next chapter presents a new reactive current reference algorithm (i.e., i_{cq}^{*}) that enables transient response enhancement of the STATCOM operating at low inverter switching frequency (i.e., 1.6 kHz).

Chapter 3 A New Reactive Current Reference Algorithm for STATCOM System Based on Cascaded Multilevel Inverters

3.1 Introduction

This chapter presents a simple decoupling feed-forward current vector controller integrating a new reactive current reference i_{cq}^{*} algorithm to enhance the transient performance of STATCOM. MCHI with separated DC capacitors driven by IPD CB-PWM technique is used to implement a single-phase STATCOM. The voltage across each DC-link capacitor is regulated by the switching pattern swapping scheme at every two fundamental frequency cycle. In this work, the STATCOM is controlled to provide both VAR compensation and grid PF correction at the PCC with a dynamically varying reactive load system. The proposed i_{cq}^{*} algorithm enhances the transient performance of the closed loop system with only P-controller and minimizes the STATCOM reactive current ripples. The single-phase STATCOM based on a five-level cascaded inverter is presented in this work and the performance of the proposed controller is investigated through various simulation studies using Matlab/Simulink software for both the steady-state and transient conditions. A laboratory prototype is also developed to verify the simulation results, where a good match between simulation and experimental results is achieved.

This chapter discusses the following: Section 3.2 describes the operating principle of the STATCOM built with MCHI along with the associated key equations and formulas. The proposed i_{cq}^{*} algorithm is explained in the third Section of this chapter. Selected simulation and experimentally validated results based on five-level cascaded inverter of the STATCOM are reported in Section 3.4. Finally the work is concluded and summarized in Section 3.5.

3.2 Multilevel Cascaded Inverter Based STATCOM

Figure 3-1 shows the single-line block diagram of the MCHI based single-phase STATCOM along with the proposed control scheme. The STATCOM is implemented by a five-level inverter (see Figure 2-4), whose

phase voltages v_c are synthesized by the summing of output voltage (i.e., $+V_{DC}$, 0, $-V_{DC}$) from each individual H-bridge inverter. Each leg of an H-bridge inverter is formed by two series-connected switching devices, which switch-on/off complementary to prevent short-circuiting the DC-link. This can be achieved by appropriate dead-band time between each switching device to ensure that either one of them is completely off before switching-on the other one.

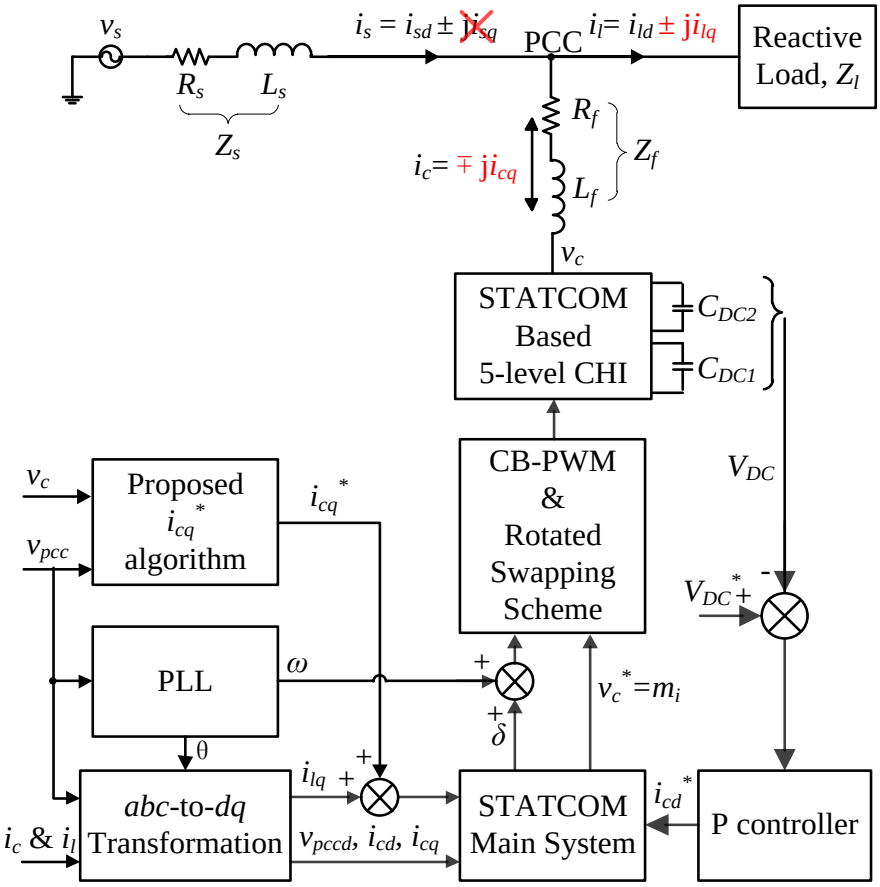


Figure 3-1. Block diagram of the single-phase STATCOM with the associated proposed control scheme.

From Figure 3-1, the STATCOM is paralleled with the power system via a series coupling inductor Z_f at the PCC [99]. The fundamental objective of the shunt VAR compensation is to reduce the voltage drop across the uncertain grid impedance Z_s, hence, increases the transmittable power along the transmission system. The amount of the reactive current i_c flowing through the coupling impedance Z_f with an impedance ratio equals to 10 (i.e., tangent^{-1}

($j\omega L_f/R_f$)) [170] is proportional to the voltage difference between the grid voltage at PCC, v_{pcc} and the STATCOM AC output voltage v_c. This can be achieved by controlling the overall magnitude of the DC-link capacitor voltages V_{DC}, hence the voltage v_c and its phase angle δ with respect to the grid voltage v_{pcc} as given by the following equation:

$$i_c = \frac{v_{pcc} - v_c \angle \pm \delta^\circ}{Z_f \angle 84.29^\circ} = i_c \angle \pm \varphi = \pm i_{cd} \pm j i_{cq} \tag{3-1}$$

where δ is the phase difference between v_{pcc} and v_c, Z_f is the coupling impedance, φ (i.e., PF angle) is the phase difference between i_c and v_{pcc}, i_{cd} is the active or real current used to charge/discharge the DC-link capacitors, and i_{cq} is the reactive current flowing through Z_f.

From Figure 3-1, PLL determines the reference phase angle θ of the grid voltage v_{pcc}, which is used to transform the load current i_{lq}, the STATCOM output voltage v_c and current i_c into dq constant vectors using the Park transformation (see Appendix B). Then, the decoupling feed-forward current vector controller (i.e., the block called “STATCOM main system” in Figure 3-1) performs feedback control and generates a set of switching signals through a dedicated modulation technique to drive the power semiconductor switches of the multilevel inverter.

Based on (3-1), the transfer function of the STATCOM link inductor in dq-coordinates is defined by:

$$\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} = \begin{bmatrix} v_{pccd} \\ v_{pccq} \end{bmatrix} - R_f \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} - L_f \frac{d}{dt} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \omega L_f \begin{bmatrix} i_{cq} \\ -i_{cd} \end{bmatrix} \tag{3-2}$$

By integrating (3-2) between current sample (k) and (k+1) and then dividing it by the operating rates (i.e., T_{id} and T_{iq} for d- and q-axis current vector controller, respectively), the average magnitude of dq-voltage vectors from the sampling period (k) to (k+1) are then derived as follows:

$$v_{cd}(k,k+1) = v_{pccd}(k,k+1) + \omega L_f i_{cq}(k,k+1) - R_f i_{cd}(k,k+1) - \frac{L_f}{T_{id}}\left[i_{cd}(k+1) - i_{cd}(k)\right] \quad (3\text{-}3)$$

$$v_{cq}(k,k+1) = -\omega L_f i_{cd}(k,k+1) - R_f i_{cq}(k,k+1) - \frac{L_f}{T_{iq}}\left[i_{cq}(k+1) - i_{cq}(k)\right] \quad (3\text{-}4)$$

Since fast and optimal current controller response is always of prime importance in STATCOM applications, therefore, the STATCOM output currents at the next sample (i.e., $i_{cd}(k+1)$ and $i_{cq}(k+1)$) are set to track the current references at the current sample (i.e., $i_{cd}^{*}(k)$ and $i_{lq}(k)$) as follows:

$$i_{cd}(k+1) = i_{cd}^{*}(k) \quad (3\text{-}5)$$

$$i_{cq}(k+1) = i_{lq}(k) \quad (3\text{-}6)$$

In order to make the variation of (3-5) and (3-6) occur linearly between the two samples (k) and (k+1) during one sampling period (i.e., k to k+1),

$$i_{cd}(k,k+1) = \frac{1}{2} i_{cd}(k) + \frac{1}{2} i_{cd}^{*}(k) \quad (3\text{-}7)$$

$$i_{cq}(k,k+1) = \frac{1}{2} i_{cq}(k) + \frac{1}{2} i_{lq}(k) \quad (3\text{-}8)$$

The grid voltage v_{pcc} and the STATCOM output voltage v_c are assumed to be constant and equal to its voltage reference within one sampling period (i.e., k to k+1) as follows:

$$v_{pccd}(k,k+1) = v_{pccd}(k) \quad (3\text{-}9)$$

$$v_{pccq}(k,k+1) = v_{pccq}(k) = 0 \quad (3\text{-}10)$$

$$v_{cd}(k,k+1) = v_{cd}^{*}(k) \quad (3\text{-}11)$$

$$v_{cq}(k,k+1) = v_{cq}^{*}(k) \quad (3\text{-}12)$$

By substituting (3-5)-(3-12) into (3-3) and (3-4), the resultant *dq*-voltage reference values are obtained as follows:

$$v_{cd}^{*}(k) = v_{pccd}(k) - R_f i_{cd}(\mathrm{k}) + \omega L_f \left[\frac{1}{2} i_{cq}(k) + \frac{1}{2} i_{lq}(k)\right] - K_{p\_id}\left[i_{cd}^{*}(k) - i_{cd}(k)\right] \tag{3-13}$$

$$v_{cq}^{*}(k) = -R_f i_{cq}(\mathrm{k}) - \omega L_f \left[\frac{1}{2} i_{cd}(k) + \frac{1}{2} i_{cd}^{*}(k)\right] - K_{p\_iq}\left[i_{lq}(k) - i_{cq}(k)\right] \tag{3-14}$$

where the proportional gain $K_{p\_i(d,q)}$ of the P-controller is given by:

$$K_{p\_i(d,q)} = \frac{L_f}{T_{i(d,q)}} + \frac{R_f}{2} \tag{3-15}$$

Hence, the desired STATCOM output voltage magnitude v_c^{*} and its phase angle δ with respect to v_{pcc} is given as follows:

$$v_c^{*} = \sqrt{(v_{cd}^{*})^2 + (v_{cq}^{*})^2} \tag{3-16}$$

$$\delta = tan^{-1}\left(\frac{v_{cq}^{*}}{v_{cd}^{*}}\right) \tag{3-17}$$

Figure 3-2 shows the implementation of the resulted STATCOM *dq*-voltage reference values given by (3-16)-(3-17).

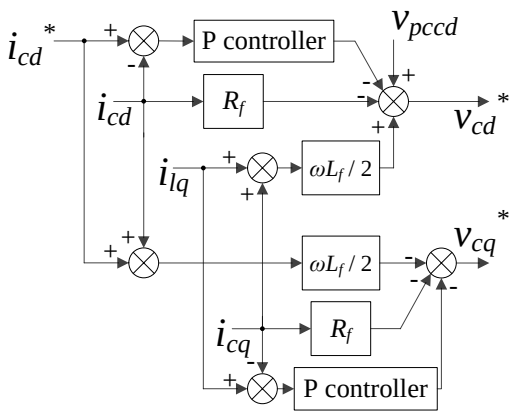


Figure 3-2. Block diagram of decoupling feed-forward current control with P-controllers.

From Figure 3-1, each separated DC-link capacitor is treated as an energy storage element to store the rectified energy via each H-bridge rectifier circuit. The sum of the DC voltage-levels V_{DC} is regulated according to the system requirement determined by the active current reference i_{cd}^{*} in the voltage loop control using a P-controller with a gain given by:

$$I_{DC} = C_{DC} \frac{dV_{DC}}{dt} \tag{3-18}$$

where I_{DC} is the current that flows through the MCHI and C_{DC} is the total DC capacitance of the two H-bridges.

Furthermore, (3-18) is defined in *dq*-coordinates as follows:

$$I_{DC\_dq} = C_{DC} \frac{dV_{DC\_dq}}{dt} \tag{3-19}$$

Since only the *d*-axis current component is required for charging and discharging the DC-link capacitors, hence, all the *q*-axis components (i.e., I_{DC_q} and V_{DC_q}) in (3-19) are neglected. By integrating (3-19) between the current sample (k) and (k+1) and then dividing it by the operating rate (i.e., T_{vd} for *d*-axis voltage vector controller), the average magnitude of active current vector from the sampling period (k) to (k+1) is therefore given by:

$$I_{DC\_d}(k,k+1) = \frac{C_{DC}}{T_{vd}} V_{DC\_d}(k,k+1) \tag{3-20}$$

The sum of the DC voltage V_{DC_d} across the DC-link capacitors at the next sample (i.e., $V_{DC\_d}(k+1)$) is set to trace the voltage reference (i.e., $V_{CD\_d}^{*}(k)$) as follows:

$$V_{DC\_d}(k+1) = V_{DC\_d}^{*}(k) \tag{3-21}$$

The current is assumed to be constant and equal to its current reference within one sampling period (i.e., k to k+1):

$$I_{DC\_d}(k,k+1) = i_{cd}^{*}(k) \tag{3-22}$$

By substituting (3-21) and (3-22) into (3-20), the resultant current reference value is then obtained as follows:

$$i_{cd}{}^{*}(k) = \frac{C_{DC}}{T_{vd}}\left[V_{DC\_d}{}^{*}(k) - V_{DC\_d}(k)\right] \tag{3-23}$$

where the DC voltage reference $V_{DC\_d}{}^{*}$ is 1 per unit (p.u.) and the proportional gain K_{p_vd} of the P-controller is given by:

$$K_{p\_vd} = \frac{C_{DC}}{T_{vd}} \tag{3-24}$$

Figure 3-3 shows the block diagram of the DC voltage feedback control described by (3-23).

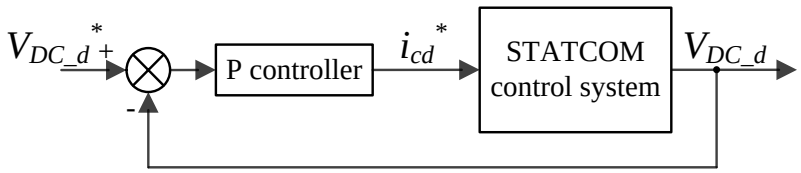


Figure 3-3. Block diagram of DC voltage feedback control with P-controller.

3.3 The Proposed External Reactive Current Reference "$i_{cq}{}^{*}$" Algorithm

Depending on the application, a STATCOM can be controlled in different modes (i.e., voltage control or flicker mitigation mode, PF mode, VAR mode, unbalance correction mode, etc.). Each mode has different sensor requirements. According to [171] and [172], the grid voltage, grid current, grid's PF as well as the STATCOM voltage, STATCOM current and STATCOM's DC voltage values are needed for the STATCOM to operate in PF or unbalance correction mode. As it can be seen from Figure 3-1 and (3-6), the extraction of the load reactive current i_{lq} is required to correct the PF of the power system. In this work, another algorithm based on the reactive current reference $i_{cq}{}^{*}$ is introduced to the decoupling feed-forward current vector controller to tackle the variation of the STATCOM output reactive current i_{cq} in DC vector quantity under the steady-state condition. This current variation/oscillation may be caused by the inverter's switching noise, non-

ideality of the components [173], unconstrained inverter switching [36], STATCOM output voltage v_c waveform distortion at low-switching frequency [174], the tolerance of DC-link capacitors, the ripple or noise content on unbalanced DC voltage, or poor transient response in the adaptive control. A well-tuned PI-controller could achieve zero steady-state error response with a minimal rise time. However, PI-controllers have some drawbacks such as maximum overshoot and high settling time (i.e., longer response and oscillation period). For instance in [48], PI-controllers were considered to provide voltage and current regulations for STATCOM based on nine-level CHI. Although good dynamic response was achieved, yet an oscillation of reactive current i_{cq} which led to poor transient response and hence, instability of the proposed system still can be obviously seen in steady-state operation. It has also been confirmed by [40] that the PI-controller may not be robust enough due to the variations of parameters and operating points, which may block the STATCOM due to the overcurrent caused by the dynamic overshoot.

Since P-controllers exhibit a rapid correction response, therefore, they have been selected and employed in this work to achieve both fast and robust control of the reactive current. The proposed i_{cq}^{*} algorithm basically provides an opposite signal to the controller in response to the variation of the STATCOM reactive current i_{cq} during the steady-state condition, hence, enhancing the transient response as well as the steady-state error without an integral function in the feedback loop. The proposed i_{cq}^{*} algorithm is derived based on the difference between the commanded voltage v_{cc}^{*}, the grid voltage v_{pccd}, and the voltage drop v_L across the coupling inductor L_f. Assuming that the STATCOM is operating in quadrant I region (see Figure 1-7) and reached steady-state, the *d*-axis current components in (3-3) and *q*-axis current components in (3-4) can be neglected as shown in Figure 3-4.

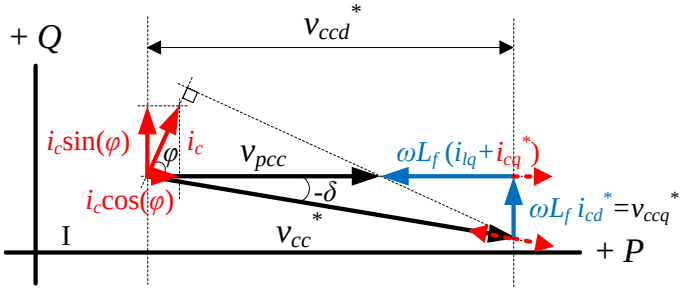


Figure 3-4. STATCOM operation in first-quadrant.

Based on Figure 3-4, the arithmetic sequence to derive the proposed i_{cq}^{*} is first illustrated as follows:

$$v_{ccd}^{*} = v_{pccd} + \omega L_f i_{lq} \tag{3-25}$$

$$v_{ccq}^{*} = \omega L_f i_{cd}^{*} \tag{3-26}$$

$$v_{cc}^{*} = 1 = \sqrt{(v_{ccd}^{*})^2 + \left(v_{ccq}^{*}\right)^2} \tag{3-27}$$

where v_{ccd}^{*} defines the resultant *d*-axis STATCOM voltage of an operating point based on the desired opposite signal $\omega L_f i_{lq}$, v_{pccd} defines the *d*-axis grid voltage, v_{ccq}^{*} defines the resultant *q*-axis STATCOM voltage of an operating point based on the resultant current reference value obtained by (3-23), and finally, v_{cc}^{*} defines the commanded voltage magnitude of the vector sum of v_{ccd}^{*} and v_{ccq}^{*}.

The command reference voltage v_{cc}^{*} is set to 1 p.u. to represent the ideal STATCOM voltage v_c (i.e., without variation) in the steady-state operating point. By referring to (3-27), the v_{ccd}^{*} in (3-25) can be re-defined as follows:

$$v_{ccd}^{*} = \sqrt{1 - \left(v_{ccq}^{*}\right)^2} \tag{3-28}$$

By substituting (3-26) into (3-28) and then equating (3-25) with (3-28), one can simply define i_{cq}^{*} as follows:

$$v_{pccd} + \omega L_f i_{lq} = \sqrt{1 - \left(v_{ccq}^{*}\right)^2} \tag{3-29}$$

$$v_{pccd} + \omega L_f i_{lq} = \sqrt{1 - \left(\omega L_f i_{cd}^{*}\right)^2} \tag{3-30}$$

$$v_{pccd}^{2} + \left(2 \times v_{pccd} \times \omega L_f i_{lq}\right) + \left(\omega L_f i_{lq}\right)^2 = 1 - \left(\omega L_f i_{cd}^{*}\right)^2 \tag{3-31}$$

$$i_{cq}^{*} = \frac{1 - \left(\omega L_f i_{cd}^{*}\right)^2 - \left(\omega L_f i_{lq}\right)^2 - v_{pccd}^{2}}{2 \times v_{pccd} \times \omega L_f} \tag{3-32}$$

And from Figure 3-4, the voltage drop v_L can then be represented as follow:

$$v_L = \sqrt{\left(\omega L_f i_{cd}^{*}\right)^2 + \left(\omega L_f i_{lq}\right)^2} \tag{3-33}$$

Hence, by substituting (3-33) in (3-32) yields the proposed reactive current reference algorithm (i.e., i_{cq}^{*}) as given in (3-34):

$$i_{cq}^{*} = \frac{1 - v_L^{\,2} - v_{pccd}^{\,2}}{2 \times v_{pccd} \times \omega L_f} \tag{3-34}$$

From (3-34), the proposed i_{cq}^{*} algorithm is equal to zero or bypassed when the grid voltage v_{pccd} is unity (i.e., PF correction provided by STATCOM based on load reactive current i_{lq}). However, due to the inverter nonlinearity [36], [50], [173], a marginal voltage difference between the grid voltage v_{pcc} and the STATCOM output voltage v_c (i.e., v_L is not equal to zero) is always appreciated specifically during the steady-state operation. To guarantee tracking of the demand signal (i.e., i_{lq}), the proposed i_{cq}^{*} algorithm is employed to trace this voltage difference and then feed-forward to the decoupling control scheme (i.e., added on top of the commanded load reactive current i_{lq}) to provide an appropriate counter reaction accordingly (i.e., minimizes the STATCOM reactive current ripples).

Figure 3-5 illustrates the block diagram of the proposed i_{cq}^{*} algorithm which is represented by (3-34).

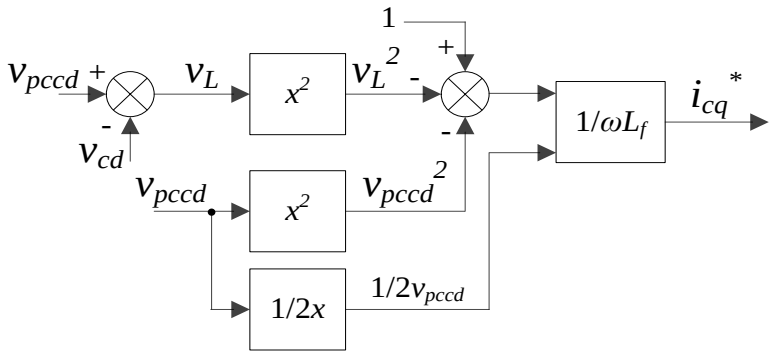


Figure 3-5. Block diagram of the proposed external reactive current reference i_{cq}^{*}.

Finally, the resultant reactive current reference i_{cq}^{*} is added to the load reactive current i_{lq} in (3-6) to form the final *dq*-voltage references as follow:

$$v_{cd}^{*}(k) = v_{pccd}(k) - R_f i_{cd}(k) + \frac{\omega L_f}{2}\left[i_{cq}(k) + \left(i_{lq}(k) + i_{cq}^{*}\right)\right] - K_{p\_id}\left[i_{cd}^{*}(k) - i_{cd}(k)\right] \quad (3\text{-}35)$$

$$v_{cq}^{*}(k) = -R_f i_{cq}(k) - \frac{\omega L_f}{2}\left[i_{cd}(k) + i_{cd}^{*}(k)\right] - K_{p\_iq}\left[\left(i_{lq}(k) + i_{cq}^{*}\right) - i_{cq}(k)\right] \quad (3\text{-}36)$$

Appendix C shows the model of the proposed control scheme implemented using Matlab/Simulink which is represented by both (3-35) and (3-36).

3.4 Results and Discussion

The single-phase STATCOM is first studied through various simulation examples using Matlab/Simulink software package [188] to investigate the effectiveness of the proposed current reference algorithm (i.e., i_{cq}^{*}). A laboratory prototype based on five-level CHI is also developed and several experiments are conducted to validate the simulation and theoretical findings. The sampling frequency of the control system is chosen to be 9.6 kHz to circumvent the task overrun situation of dSPACE DS1104 controller board [175]. IPD CB-PWM technique with an effective switching frequency of 1.6 kHz (see model in Appendix D) is considered as a modulation technique for the CHI.

3.4.1 Simulation Results

The single-phase STATCOM is investigated with the circuit diagram depicted in Figure 3-6 and the system parameters tabulated in Table 3-1. The fundamental switching time (i.e., 0.02 second) is selected for both the T_{id} and T_{vd} in (3-13) and (3-24), respectively, while T_{iq} is set to be 0.002 second to avoid large resultant gain which can lead to system instability. The coupling resistor R_f and inductor L_f as given in (3-38) and (3-39), respectively, are obtained by equating the impedance ratio of the coupling impedance Z_f to 10 (i.e., tangent^{-1} ($j\omega L_f/R_f$) or see (3-37)) in order to emulate the real-world transmission line impedance [170].

$$\frac{X_f}{R_f} = 10 \tag{3-37}$$

$$Z_f = \sqrt{R_f{}^2 + X_f{}^2} = \frac{v_{pcc}}{i_c} = \frac{240}{6} = 40\,\Omega$$

$$R_f{}^2 = Z_f{}^2 - X_f{}^2 = 40^2 - 10^2 R_f{}^2 \tag{3-38}$$

$$101 R_f{}^2 = 40^2$$

$$R_f = 4\,\Omega$$

$$L_f = \frac{X_f}{2\pi f} = \frac{10 \times R_f}{2\pi f} = \frac{10 \times 3.98}{2\pi \times 50} = 127\,\text{mH} \tag{3-39}$$

Table 3-1. System Parameters Used in Computer Simulation and Practical Experiment.

Symbol	Quantity	Value
S_{base} = 1.44 kVA, V_{base} = 240 Vrms, I_{base} = 6 Arms, Z_{base} = 40Ω		
f	Fundamental frequency	50 Hz
f_{sw}	Switching frequency	1.6 kHz
f_s	Sampling frequency	9.6 kHz
v_{pcc}	Grid voltage	240 V_{rms} = 1 p.u.
R_s	Grid resistor	0.4 mΩ = 0.01 p.u.
L_s	Grid inductor	12.7 mH
Z_s	Grid impedance	4 Ω = 0.1 p.u.
R_f	Coupling resistor	4 Ω = 0.1 p.u.
L_f	Coupling inductor	127 mH
Z_f	Coupling impedance	40 Ω = 1 p.u.
R_{l_A}	Load A resistor at 0.67 lagging PF	60 Ω = 1.5 p.u.
L_{l_A}	Load A inductor at 0.67 lagging PF	190 mH
Z_{l_A}	Load A impedance	85 Ω = 1.4 p.u.
i_{l_A}	Load A current	4 A_{rms} = 0.67 p.u.
R_{l_B}	Load B resistor at 0.67 leading PF	60 Ω
C_{l_B}	Load B capacitor at 0.67 leading PF	53 μF
Z_{l_B}	Load B impedance	85 Ω = 1.4 p.u.
i_{l_B}	Load B current	4 A_{rms} = 0.67 p.u
C_{DCM}	DC capacitance of M^{th} H-bridge (i.e., M =1, 2)	1000 μF
C_{DC}	Total DC capacitance of the H-bridges	500 μF
K_{p_vd}	d-axis voltage gain	0.25
K_{p_id}	d-axis current gain	0.21
K_{p_iq}	q-axis current gain	1.63

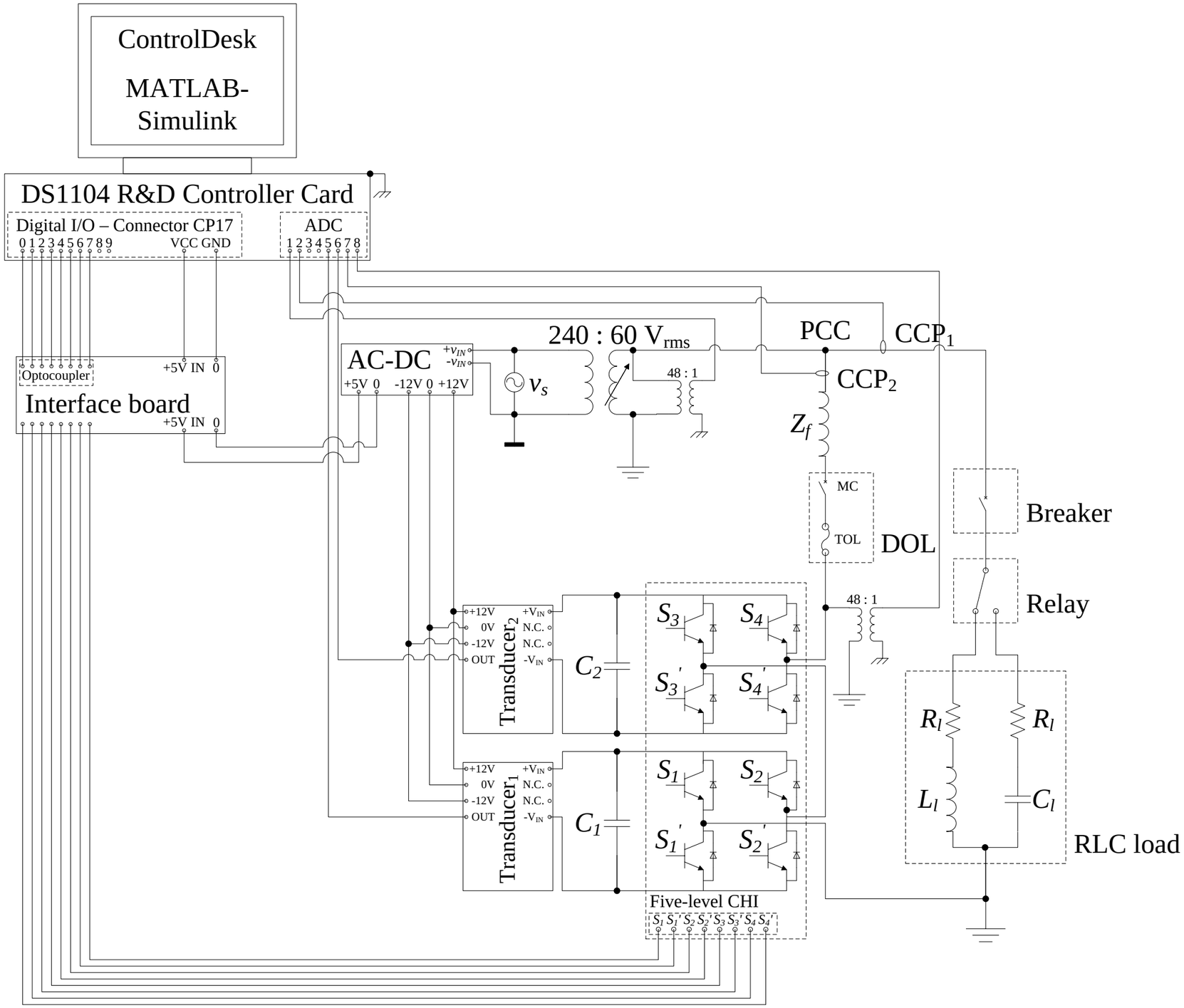


Figure 3-6: Circuit diagram of five-level H-bridge inverter based single-phase STATCOM with separated DC capacitors.

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Furthermore, the inductive load R_lL_l and capacitive load R_lC_l with 0.67 lagging and leading PF, respectively, are obtained as follows:

$$\text{PF} = \frac{P_l}{Z_l} = 0.67 \tag{3-40}$$

$$P_l = \text{PF} \times S_l = 0.67 \times 1440 = 960\,\text{W} = Q_l \tag{3-41}$$

$$R_l = \frac{v_s^{\,2}}{P_l} = \frac{240^2}{960} = 60\,\Omega \tag{3-42}$$

$$L_l = \frac{X_l}{2\pi f} = \frac{60}{2\pi \times 50} = 190\,\text{mH} \tag{3-43}$$

$$C_l = \frac{1}{X_c \times 2\pi f} = \frac{1}{60 \times 2\pi \times 50} = 53\mu\text{H} \tag{3-44}$$

The STATCOM system's dynamics, steady-state, and transient scenarios are analysed with different loading conditions. The simulation study (see model in Appendix E) was carried out with linear single-phase reactive load which changes from R_lL_l to R_lC_l characteristic (i.e., from lagging to leading PF) at the time of 1 second.

Figure 3-7 illustrates the performance of the STATCOM in response to a step change in the load.

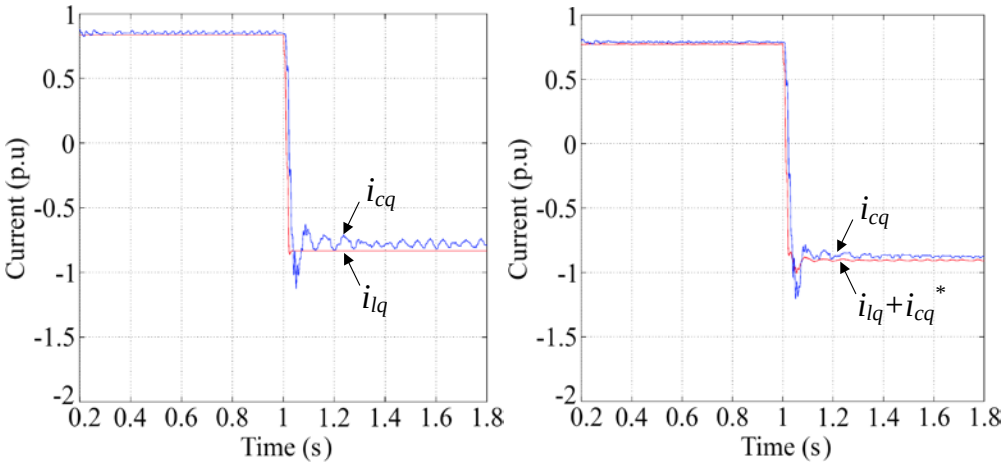
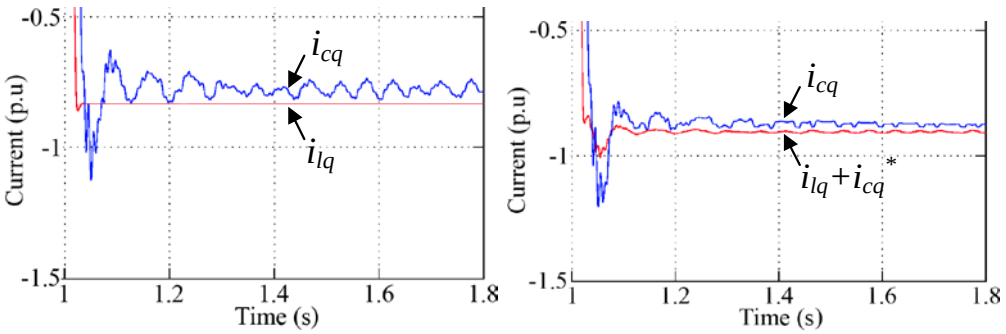


Figure 3-7. Simulation results of step change in the load current i_{lq} and STATCOM reactive current i_{cq} (a) without and (b) with the proposed i_{cq}^* algorithm.

Specifically, Figure 3-7(a) presents the dynamic response of the STATCOM reactive current i_{cq} without the proposed i_{cq}^* algorithm and Figure 3-7(b) shows the characteristic of the STATCOM reactive current i_{cq} with the proposed current references (i.e., $i_{lq} + i_{cq}^*$).

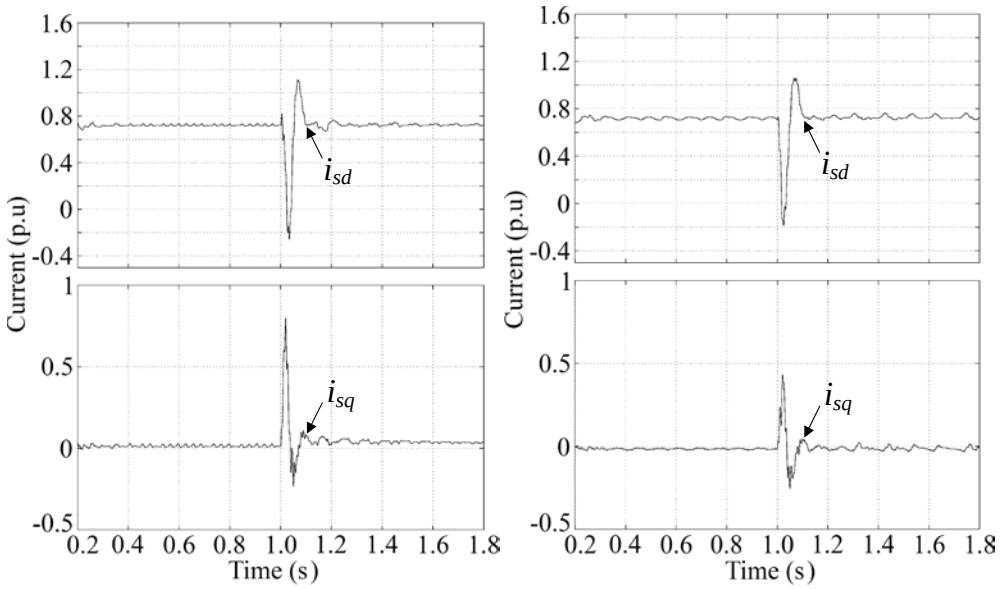
A closer "zoomed" look of Figure 3-7 is also presented in Figure 3-8 where it is clearly shown that the steady-state error and transient response of the STATCOM incorporating the proposed i_{cq}^* algorithm to the step change of the load is greatly improved while achieving fast system response (see Figure 3-7(b)). Furthermore, it is worth noticing that with the proposed i_{cq}^* algorithm, the variation/oscillation of the measured STATCOM reactive current i_{cq} is mitigated without implementing any filtering circuit.



(a) (b)

Figure 3-8. Close-up view of Figure 3-7 (a) without and (b) with the proposed i_{cq}^* algorithm.

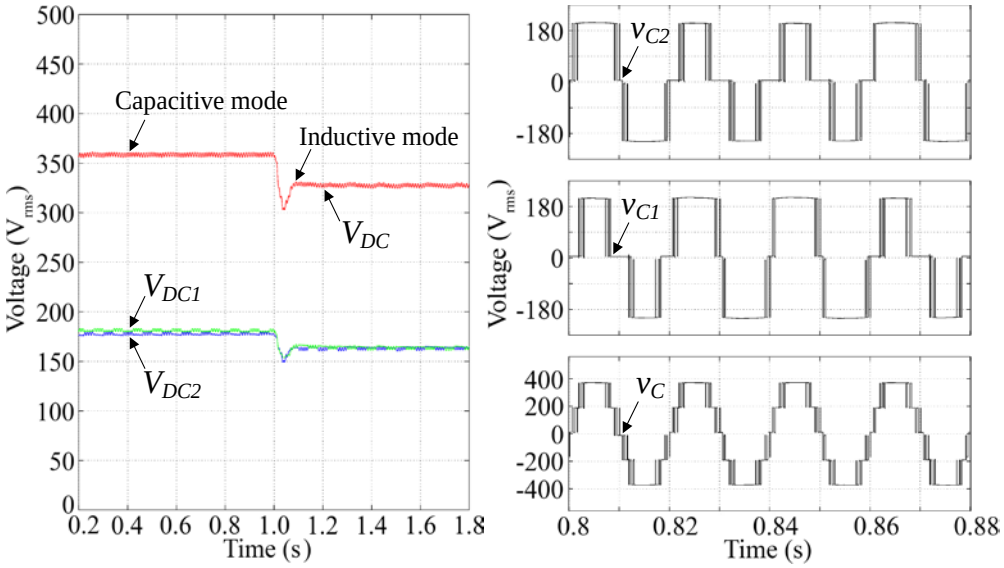
As PLL requires a processing delay of at least half of the fundamental cycle for the STATCOM output voltage v_c to be synchronized with the new voltage v_{pcc}'s phase angle θ, the effect of this delay on the grid current i_s during the change in the load condition is demonstrated in Figure 3-9. This leads to VAR exchange occurs between the STATCOM and the transmission lines and therefore, causing the STATCOM to exhibit one or more oscillations or spikes (see Figure 3-8(a)) when the load is changed. The cause of this phenomenon can be observed from Figure 3-9(a) on both the grid active i_{sd} and reactive i_{sq} currents. However, as shown in Figure 3-9(b), when the proposed i_{cq}^* algorithm is introduced to the decoupling feed-forward current vector controller, the spikes in the grid reactive current i_{sq} is considerably reduced by 50%.



(a) (b)

Figure 3-9. Simulation results of the grid active current i_{sd} and reactive current i_{sq} (a) without and (b) with the proposed i_{cq}^{*} algorithm.

The dynamic and transient responses of the total DC-link capacitor voltage's (i.e., V_{DC}) controller in response to inductive and capacitive VAR generations are demonstrated in Figure 3-10(a) while Figure 3-10(b) presents the three-level AC output voltages generated from each H-bridge inverter level and the overall five-level STATCOM output voltage v_c.



(a) (b)

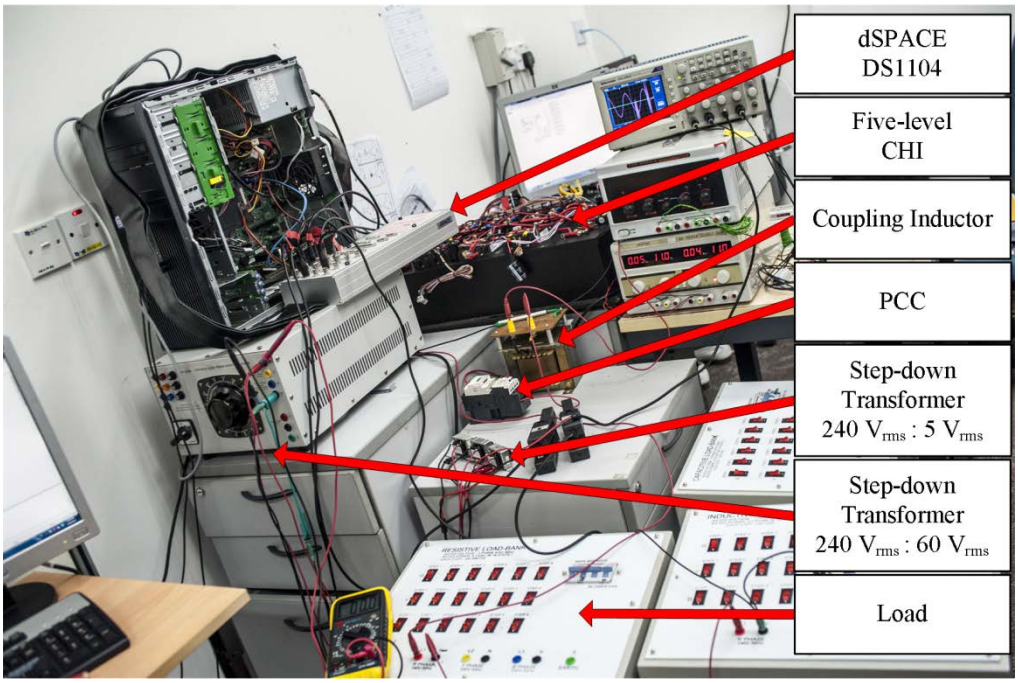
Figure 3-10. Simulation results of (a) the total DC link capacitor voltages V_{DC} with the proposed i_{cq}^{*} and (b) the five-level cascaded voltage waveform

generated via the IPD CB-PWM technique with switching pattern swapping scheme.

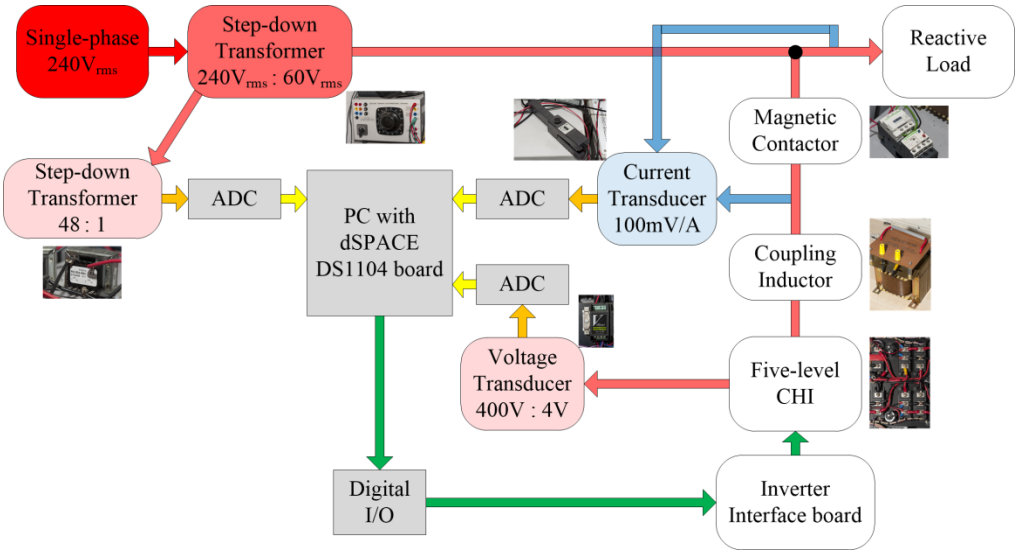
Figure 3-10(a) shows that the DC voltage-level across each DC-link capacitor is maintained constant using the switching pattern swapping scheme. This ensures equal switching stresses, conduction losses, and power handling between the H-bridges. Moreover, the scheme assists the control system to response quicker during the step changes of load reactive current. According to (3-1), it is revealed that when the DC peak voltage-level V_{DC} is higher than the grid peak voltage v_{pcc}, the STATCOM is operating in a capacitive mode to deliver reactive current to the power system. In contrast, when the STATCOM operates in an inductive mode, the DC peak voltage-level V_{DC} is lower than the grid voltage v_{pcc} to absorb reactive current from the power system. From Figure 3-10(b), the switching patterns are swapped between the H-bridge inverters at every two fundamental frequency cycle to resolve the current imbalance stress [176]. However, the five-level output voltage waveform still can be correctly obtained on the AC side of the cascaded inverter.

3.4.2 Experiment Results

A laboratory prototype based on a single-phase STATCOM (see Figure 3-6 and Figure 3-11) with the system parameters tabulated in Table 3-1 is developed and tested to validate the theoretical and the simulation findings. From Figure 3-11, a dSPACE DS1104 processor board with CLP1104 connector panels is used as the main control platform. It enables the linkage between the analogue and digital interface by introducing the Input-Output (I/O) interface blocks into the Matlab/Simulink model. With the Matlab/Simulink real-time workshop function, the Matlab/Simulink model with the dSPACE interface blocks are automatically converted into C-code, compiled, and then linked to the real-time dSPACE DS1104 processor board for digital signal processing. The application of the dSPACE Graphical User Interface (GUI) software allows the user to alter and monitor the model behaviour as well as the control parameters in real-time.



(a)



(b)

Figure 3-11. (a) Experimental set up and (b) block diagram of analogue components arrangement of the single-phase (one-leg) STATCOM system based on the five-level CHI with separated DC capacitors.

Two step-down transformers (i.e., Multicomp MCF/B1805F) with turns ratio of 48:1 (i.e., 240 V_{rms} : 5 V_{rms}) are used to scale down the measured grid voltage v_{pcc} and STATCOM voltage v_c to a safe and workable voltage-level for the dSPACE DS1104 controller board. Two current clamp-on probes (CCP) (i.e., Tektronix A622) are used to measure both the load current i_l and

the STATCOM output current i_c. A digital real-time oscilloscope (OSC) (i.e., Tektronix TDS2004C) with four channels is used to capture and display the selected output voltage and current waveforms simultaneously. The two H-bridge inverter cells are constructed using IGBT modules (MG75J6ES50 from Toshiba) and they are connected together in series to form a phase-leg of five-level CHI. A coupling inductor L_f rated at 6 A_{rms} is connected in series with the inverter prior to the PCC via an electro-Magnetic Contactor (MC) protected with a 6 A_{rms} Thermal Overload Relay (TOR). The MC is manually controlled to connect and disconnect the single-phase STATCOM system at the PCC by separate start and stop push buttons, respectively. An auxiliary contact on the MC is connected across the start button as a hold-in contact to electrically latch closed the MC when the start button is pressed. This method is known as Direct-On-Line (DOL) starter as represented in the wiring diagram of Figure 3-12.

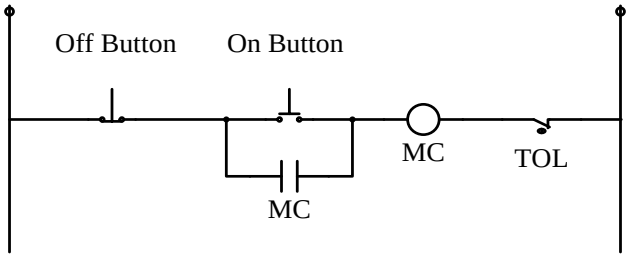
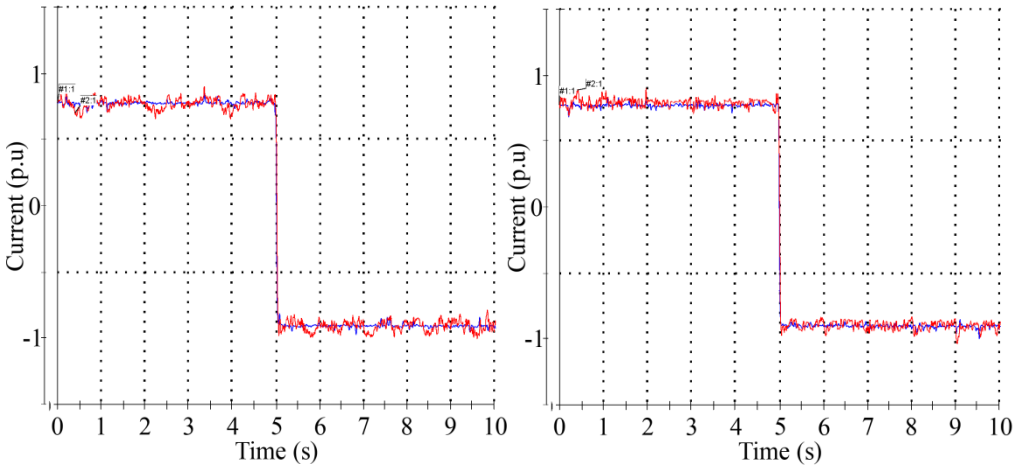


Figure 3-12. Wiring diagram of DOL starter.

To verify the real-time performance of the proposed i_{cq}^* algorithm, the STATCOM system is set to operate in both the capacitive and inductive modes at 1 kVA for 10 seconds. The selected experimental results are analysed for PF correction, system dynamic, steady-state, and transient response. Multiple plotter instruments from the dSPACE controldesk's element library under "Data Acquisition" group are utilized to monitor the behaviour of the control variables.

Specifically, Figure 3-13 shows the dynamic response of the STATCOM current tracking characteristics in response to a step change in the reactive current reference from inductive to capacitive, which occurred at the 5^{th} second. A good dynamic characteristic with an instantaneous response is observed in Figure 3-13. In addition, mitigation of the STATCOM current i_{cq}

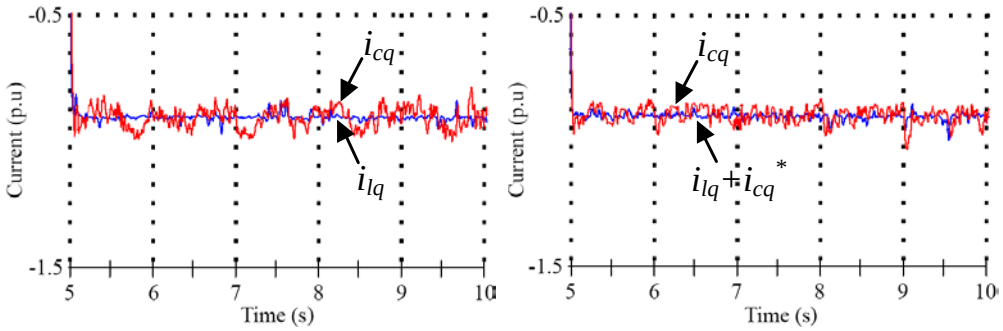
variation with the application of the proposed i_{cq}^* algorithm is achieved (see Figure 3-13(b)) without scarifying the speed and the precision of the controller.



(a) (b)

Figure 3-13. Experiment waveforms of load and STATCOM reactive currents during the reactive loads transition (a) without and (b) with the proposed i_{cq}^* algorithm.

This can be clearly seen from the closer "zoomed" view of the STATCOM reactive current i_{cq} during the capacitive compensation (i.e., from 5 to 10 seconds) presented in Figure 3-14.



(a) (b)

Figure 3-14. Close-up view of Figure 3-13 (a) without and (b) with the proposed i_{cq}^* algorithm.

Figure 3-15 shows the individual DC-link voltage waveform of each H-bridge inverter (i.e., V_{DC1} and V_{DC2}) and the total DC voltages of phase-leg (i.e., V_{DC} = V_{DC1} + V_{DC2}) when the STATCOM system is changed from capacitive to inductive mode at the 5th second.

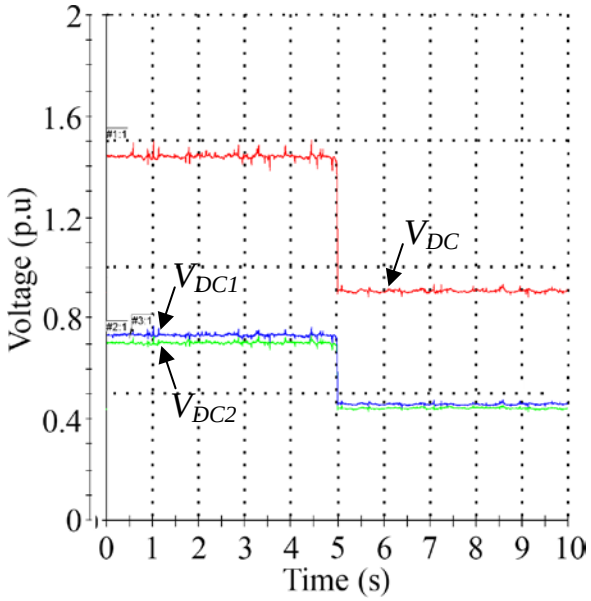
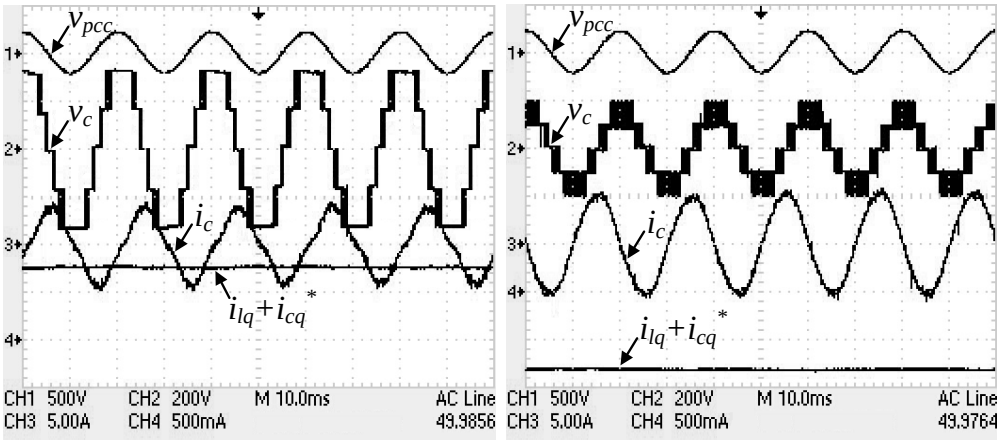


Figure 3-15. Experimental waveforms of each and total DC-link capacitors' voltages V_{DC} with the proposed i_{cq}^{*} algorithm and switching pattern swapping scheme during the reactive loads transition.

With the switching pattern swapping scheme incorporated with the IPD CB-PWM technique, the DC-link voltages are balanced and eventually become equal. It can also be observed that the DC voltage V_{DC} is higher when the STATCOM system is operating in capacitive mode to compensate the inductive load A and it is vice-versa when the STATCOM system is operating in an inductive mode to compensate the capacitive load B.

Figure 3-16 presents the experimental waveforms (i.e., from top to bottom) of the grid voltage v_{pcc}, the five-level STATCOM output voltage v_c, the STATCOM output current i_c, and the reactive current references (i.e., i_{lq} + i_{cq}^{*}), respectively, for both capacitive and inductive modes. When the STATCOM is operating in capacitive mode (see Figure 3-16(a)), the voltage v_c exceeds and lags the grid voltage v_{pcc} to compensate the inductive load A. Since the direction of the current probe was pointing towards the PCC, a lagging STACOM reactive current i_{cq} is observed as shown in Figure 3-16(a). On the other hand, Figure 3-16(b) shows the operation of the STATCOM in the inductive mode, where the voltage v_c waveform is lower and leads the grid voltage v_{pcc} to compensate the capacitive load B. This produces a leading STATCOM reactive current i_{cq} flowing through the coupling inductor L_f and

towards the PCC. Furthermore, it is worth noting that low-order harmonics start to appear in the capacitive mode due to the pulse drop (see Figure 3-16(a)) as the inverter is driven into the overmodulation region (i.e., m_i > 1 p.u.).



(a) (b)

Figure 3-16. Experimental waveforms (channel 1: grid voltage v_{pcc}, channel 2: five-level STATCOM output voltage v_c, channel 3: the STATCOM output current i_c, channel 4: the reactive current references (i.e. i_{lq} + i_{cq}^*), when the STATCOM is operating in (a) capacitive mode and (b) inductive mode at 1 kVA.

3.5 Summary

The proposed new reactive current reference i_{cq}^* algorithm suitable for STATCOM system was described in this chapter. For simplicity, five-level inverter was used to construct the single-phase STATCOM. The performance of the proposed method was investigated through simulation and experimental studies. The algorithm has demonstrated its ability to achieve good transient response for VAR compensation under different loading conditions without using any integral functions and filters in the feedback control loop. Rotated switching swapping scheme was employed to balance the DC-link capacitor voltages and hence equalize the current stress through switching devices. Interestingly, the proposed i_{cq}^* algorithm was also able to minimize the effect of the inherent PLL delay which normally causes the STATCOM to exhibit large oscillations. The measured STATCOM current i_{cq} was very close to the current reference values and showed a reasonably smooth profile when the proposed i_{cq}^* algorithm is integrated into the system. Thus, reduces the

problem of voltage instability and enhances the overall system performance.

The next chapter extends the application of the proposed control scheme to the MCHI based single-phase STATCOM driven by MSHE-PWM technique with variable DC voltage-levels.

Chapter 4 SHE-PWM Cascaded Multilevel Inverter with Adjustable DC-Voltage Levels Control for STATCOM Applications

4.1 Introduction

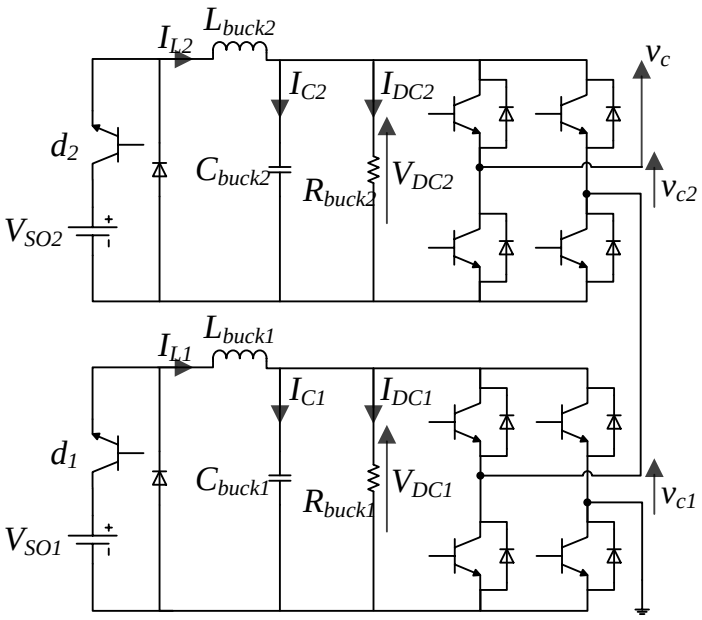
This chapter presents a new MSHE-PWM technique (i.e., proposed by Dahidah et al. [98]) for transformer-less STATCOM system based on MCHI configuration. The proposed MSHE-PWM method optimizes both the DC voltage-levels and the switching angles, enabling more harmonics to be eliminated (i.e., (N+M)-1 as opposed to N-1) without sacrificing the structure of the inverter circuit. This method interestingly provides constant switching angles and linear pattern of DC voltage-levels over the m_i range that eliminates the tedious steps required for the off-line calculation of the switching angles; therefore, easing the implementation of the MSHE-PWM for dynamic systems. As the new method solely relies on the availability of the variable DC voltage-levels, the rapid development of power semiconductor technologies has led to produce high-efficiency DC-DC converters; hence, for simplicity, buck- and boost-type converter are considered in this chapter for that purpose. The proposed control scheme (i.e., from Chapter 3) and voltage closed loop controllers are implemented for both the STATCOM and the DC-DC converters, respectively, to meet the VAR demand at different loading conditions. In this chapter, the MSHE-PWM is first compared to the IPD CB-PWM technique operating with the same switching frequency to illustrate its enhanced characteristics. Then, the investigation is extended by exploring the STATCOM performance based on the new variation of MSHE-PWM technique with different distribution ratios (i.e., the number of constant quarter-cycle switching angles/transitions; case I: N_1/N_2 = 3/5 and case II: N_1/N_2 = 3/8). The effectiveness and the theoretical analysis of the proposed approach are verified through both simulation and experimental studies.

This chapter discusses as following: Section 4.2 presents the analysis and the formulation of the proposed method applied to five-level SHE-PWM inverter. Section 4.3 addresses the STATCOM system configuration and the controllers for the DC-DC converters. Selected simulation and experimentally

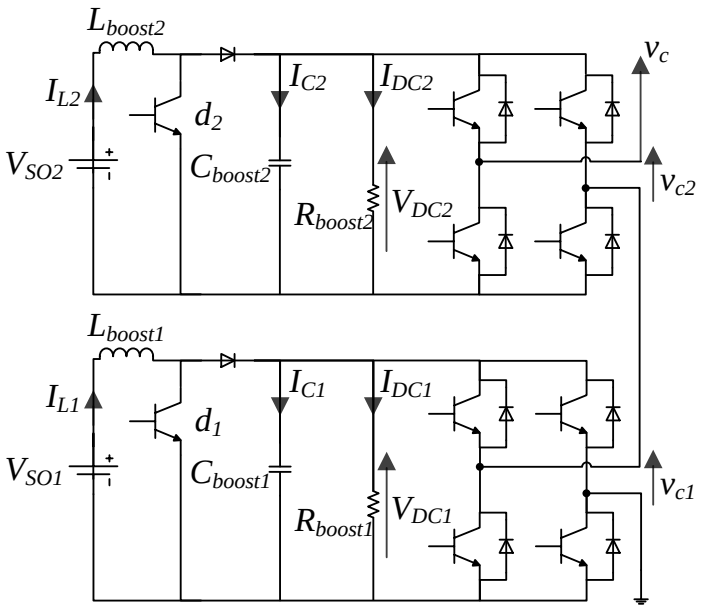
validated results are reported in Section 4.4. Finally, conclusions are summarized in Section 4.5.

4.2 Five-Level SHE-PWM with Variable DC Voltage-Levels

The proposed single-phase five-level voltage source CHI with separated DC-DC buck- and boost-type converters are shown in Figure 4-1(a) and Figure 4-1(b), respectively.



(a)



(b)

Figure 4-1. Single-phase two cascaded H-bridges with separated DC-DC (a) buck and (b) boost converters.

The parameters of the converters shown in Figure 4-1 (see Appendix F for buck converter and Appendix J for boost converter) are tabulated in Table 4-1.

Table 4-1: Converter Parameters Used in the Simulation Study.

Quantity	DC-DC buck converter	DC-DC boost converter
DC voltage source V_{SO}	240 V	60 V
Filter inductor L	0.5 mH	6.4 µH
Filter capacitor C	0.25 mF	300 µF
Switching frequency f_{sw}	2 kHz	25 kHz

The reason of implementing these two DC-DC converter topologies is to discover the advantage of each one based on the same voltage closed loop controller design using the state-space averaging modelling technique. In many applications, it is important for a converter/inverter to be lightweight and of a relatively small size [177]. From Table 4-1, the boost converter is no doubt the favourable one when compared to the buck converter due to its smaller size of $L_{boost}C_{boost}$ output filter possessed by high switching frequency.

Although the proposed work relies on the operation of DC-DC converters, it is worth noting that any converter could be equally applied as long as it satisfies its purpose in providing the “fluctuation-free” variable DC voltage-levels to the inverter cells. For a commercial STATCOM which specifically designed for PF or unbalance compensation, typically there is an “optional” ESS which serves the purpose of storing electrical power received from a generating station (i.e., wind farm, solar panels) or from the AC grid network [171], [172]. Thus, this ESS can be served as the DC voltage souce V_{SO} for the converters.

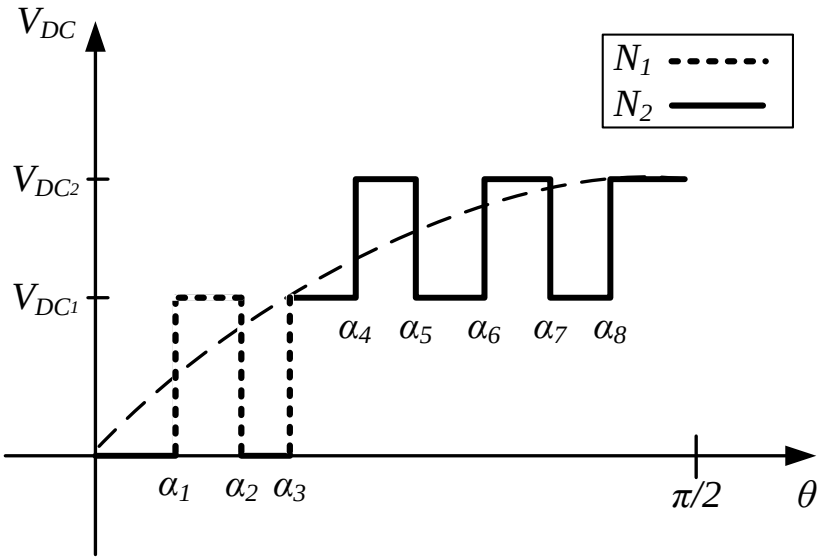
Besides that, including extra DC-DC converters will not deteriorate the practicability and the performance of the STATCOM system as relatively medium- to high-voltage DC-DC converters with high switching frequencies ranges from 5 kHz [179] to 50 kHz [180] have been proposed by several recent research articles for different applications including grid-connected converters, PV integration with the grid, etc. [179]-[184]. For instance, Akagi and Kitada [182] proposed high-voltage (i.e., 6.6 kV) modular multilevel

cascaded back-to-back inverter combining bidirectional isolated DC-DC converter operating at switching frequency of 20 kHz. Nevertheless, the buck converter employed in this work is operated with a switching frequency of only 2 kHz, which considered acceptable as suggested by enormous recent literature in the field.

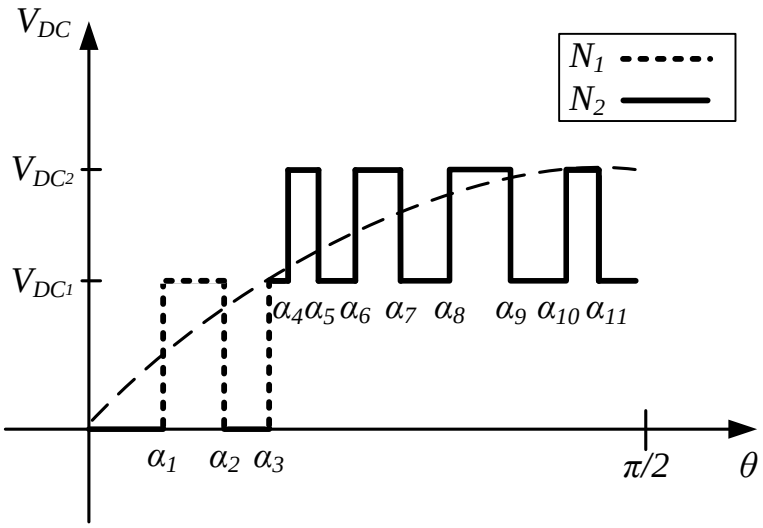
Furthermore, electrical isolation for the DC-DC stage can be achieved by employing high-frequency transformer due to its higher degree of efficiency (i.e., through reduction of transformer losses when compared to 50 Hz transformer) as well as light and compact size [177], [178]. However, due to the extremely low resistance of the winding turns, the high frequency transformer is not able to cope with the volt-second asymmetry/inequality problem; therefore, pushing its core materials into saturation (i.e., resulting unwanted departure from ideal behaviour caused by the generation of harmonics and intermodulation distortion). Nevertheless, an elegant solution for the full-bridge converter has been demonstrated in [177] using the current mode control (i.e., rather than putting a small air-gap in series with the core) to control the asymmetry problem.

In this chapter, the constant quarter-cycle switching angles with a distribution ratio of N_1/N_2 = 3/5 and N_1/N_2 = 3/8 are assumed to construct the five-level SHE-PWM waveform as shown in Figure 4-2(a) and Figure 4-2(b), respectively. The target in each case is to eliminate nine (i.e., 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, and 29^{th}) and twelve (i.e., 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th}, 31^{st}, 35^{th}, and 37^{th}) low-order non-triplen harmonics, respectively, while controlling the fundamental component at pre-defined value.

From Figure 4-2, it is worth noting that the constant quarter-cycle switching angles for Case I and Case II make the effective switching frequency of the inverter equals to 1.6 kHz (i.e., 32×50 Hz) and 2.2 kHz (i.e., 44×50 Hz), respectively. Therefore, when compared to the CB-PWM based STATCOM with a typical switching frequency ranges between 5 kHz [154] and 10 kHz [185], the proposed MSHE-PWM method offers considerably less losses, less cooling, and low power dissipation requirement, which could largely reduce the volume and the weight of overall system and hence, increase its reliability and performance.



(a)



(b)

Figure 4-2. Five-level SHE-PWM waveform with a distribution ratio of (a) Case I: N_1/N_2 = 3/5 and (b) Case II: N_1/N_2 = 3/8 (only quarter-cycle shown).

The STATCOM output voltage waveform is described by Fourier series (4-1) and the optimal switching angles and the DC voltage-levels are obtained by solving the following objective function when it is subject to the constraints of (4-2) and (4-3).

$$\left(V_{DC_1} \sum_{l=1}^{N_1} (-1)^{l+1} \cos(\alpha_l) + V_{DC_2} \sum_{l=N_1+1}^{N_1+N_2} (-1)^{l} \cos(\alpha_l) \right) = \frac{m_l \times \pi}{4}$$

$$\left(V_{DC_1} \sum_{\iota=1}^{N_1} (-1)^{\iota+1} \cos\left(5\alpha_\iota\right) + V_{DC_2} \sum_{\iota=N_1+1}^{N_1+N_2} (-1)^{\iota} \cos\left(5\alpha_\iota\right) \right) = 0$$

$$\vdots$$

$$\left(V_{DC_1} \sum_{\iota=1}^{N_1} (-1)^{\iota+1} \cos\left(n\alpha_\iota\right) + V_{DC_2} \sum_{\iota=N_1+1}^{N_1+N_2} (-1)^{\iota} \cos\left(n\alpha_\iota\right) \right) = 0 \quad (4\text{-}1)$$

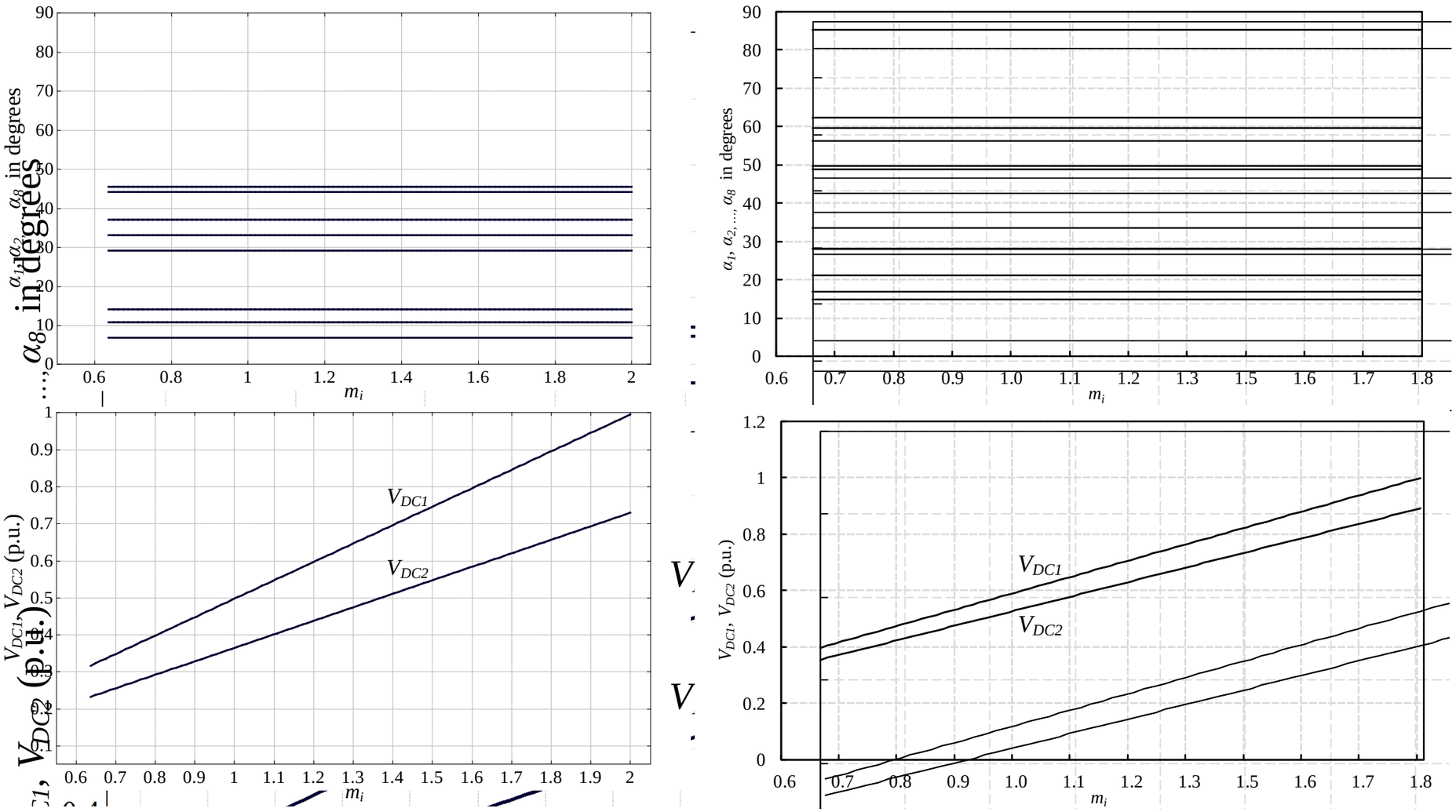
where N_1 is the number of switching transitions between zero- and the first-level which must be an odd number, N_2 is the number of switching transitions between the first-level and the second-level which can be either odd or even number, and m_i is the modulation index.

$$\left(0 < \alpha_\iota < \alpha_2 < \ldots < \alpha_{N_1+N_2} < \frac{\pi}{2} \right) \quad (4\text{-}2)$$

$$V_{DC\_min} \le V_{DC_M} \le V_{DC\_max} \quad (4\text{-}3)$$

where V_{DC_min} and V_{DC_max} are the minimum and maximum values of the DC voltage source, respectively and V_{DCM} is the M^{th} DC voltage-level (i.e., M =1, 2).

The constraints (i.e., (4-2) and (4-3)) are imposed in the formulation to ensure that the resultant waveform is realizable and physically correct. Specifically, (4-3) assures that the optimal DC-level is within a certain range. An optimization technique based on the approach proposed in [91] and [98] is employed to find the solution of (4-1) and multiple sets of solutions for various multilevel waveforms with different distribution ratios and different ranges of m_i were obtained. However, only two sets of solutions (i.e., Case I: N_1/N_2 = 3/5 and Case II: N_1/N_2 = 3/8) are presented in this chapter as depicted in Figure 4-3 while more solutions for the same multilevel waveforms can be found in [98].



(a) (b)

Figure 4-3. Switching angle and DC voltage-levels solution for five-level waveform with (a) N = 3/5, 0.64 < m_i <2.0 and (b) N = 3/8, 0.63 < m_i <1.8.

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4.3 The Proposed Single-Phase STATCOM: Key Operation

Figure 4-4 shows the single-line block diagram of the proposed five-level SHE-PWM inverter based single-phase STATCOM system and the associated proposed control schemes.

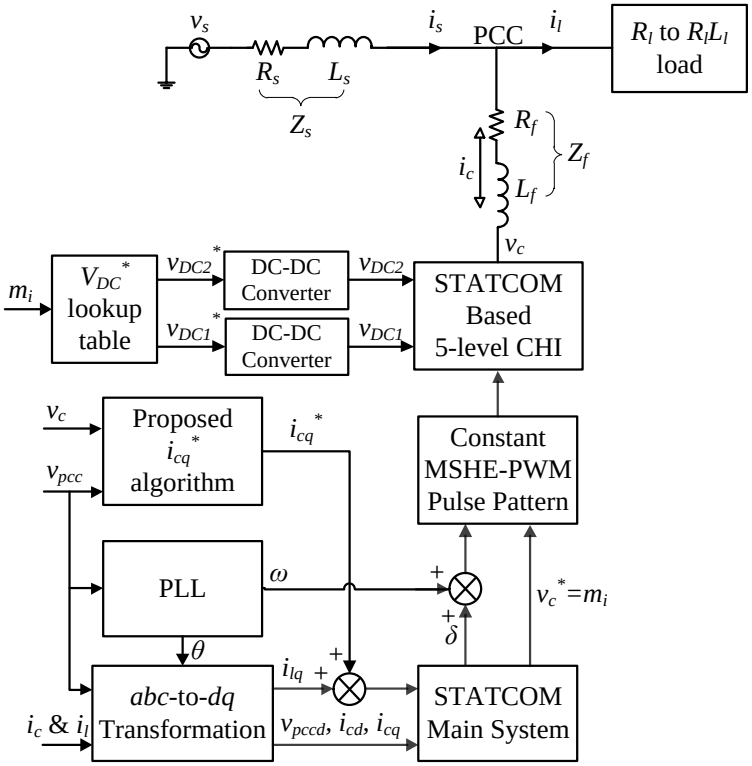

Figure 4-4. Block diagram of the single-phase STATCOM system with the associated proposed control scheme.

From Figure 4-4, the STATCOM is paralleled with the power system via a coupling inductor Z_f at the PCC. The decoupling feed-forward current vector controller integrating with the proposed i_{cq}^* algorithm (i.e., from Chapter 3) is employed in this chapter, where the resultant *dq*-voltage reference values are given as:

$$v_{cd}^*(k) = v_{pccd}(k) - R_f i_{cd}(k) + \frac{\omega L_f}{2}\left[i_{cq}(k) + \left(i_{lq}(k) + i_{cq}^*\right)\right] - K_{p\_id}\left[-i_{cd}(k)\right] \tag{4-4}$$

$$v_{cq}^*(k) = -R_f i_{cq}(k) - \frac{\omega L_f}{2}\left[i_{cd}(k)\right] - K_{p\_iq}\left[\left(i_{lq}(k) + i_{cq}^*\right) - i_{cq}(k)\right] \tag{4-5}$$

where v_{pccd} defines the *d*-axis grid voltage, R_f and L_f are the coupling resistor and inductor, respectively, ω defines the fundamental grid voltage frequency, i_{cd} and i_{cq} are the active and reactive current of the STATCOM, respectively, i_{cq}^* is the proposed reactive current reference algorithm, and i_{lq} is the reference reactive current extracted from the load side.

From (4-4) and (4-5), the respective proportional gain $K_{p\_i(d,q)}$ of the P-controller is given by:

$$K_{p\_i(d,q)} = \frac{L_f}{T_{i(d,q)}} + \frac{R_f}{2} \tag{4-6}$$

where T_i defines the controller operating rate.

The desired STATCOM output voltage magnitude v_c^* and its phase angle δ with respect to v_{pcc} is given as follows:

$$v_c^* = \sqrt{(v_{cd}^*)^2 + (v_{cq}^*)^2} \tag{4-7}$$

$$\delta = tan^{-1}\left(\frac{v_{cq}^*}{v_{cd}^*}\right) \tag{4-8}$$

The real-time implementation of the proposed control scheme model (see (4-4) and (4-5)) using Matlab/Simulink is shown in Appendix C.

The proposed MSHE-PWM method relies on the availability of the variable DC voltage-levels which can be easily obtained by DC-DC converters. With the rapid growth in semiconductor devices industry and advanced materials such as nanocrystalline soft magnetic core that offers high saturation flux density (more than 1.2 T) and high relative permeability (in the 10000 to 100000 range) leading to an extremely low core loss, the combination of the magnetic core with the latest trench-gate IGBTs and super-junction MOSFETs has made it possible to improve the system efficiency of the DC-DC converters up to 97% or higher [186]. In the near future, the emergence of SIlicon Carbide (SiC) switching devices and a new magnetic core material will allow the system efficiency to reach higher than 99% [153].

To illustrate the feasibility of the proposed MSHE-PWM method and for simplicity, a DC-DC buck- and boost-type converter which operates at

only 2 kHz and 25 kHz, respectively, are considered in this chapter to provide the variable DC voltage-levels for each H-bridge inverter according to the operating point (i.e., m_i).

4.3.1 DC-DC Buck Converter

With the assumption of ideal components (i.e., switch, capacitor C_{buck}, and inductor L_{buck}), the voltage closed loop controller for the buck converter is designed in Continuous Conduction Mode (CCM) by using the state-space averaging modelling technique with Venable approach [187]. The state-space equation of the buck converter for mode 1 (i.e., switch is on) and mode 2 (i.e., switch is off) are defined in (4-9) and (4-10), respectively.

$$\begin{bmatrix} \frac{dI_L}{Dt} \\ \frac{dV_{DC}}{Dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{buck}} & -\frac{1}{R_{buck}C_{buck}} \end{bmatrix} \begin{bmatrix} I_L \\ V_{DC} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{SO} \rightarrow \frac{dX}{Dt} = [A_1][X] + [B_1]U \tag{4-9}$$

$$\begin{bmatrix} \frac{dI_L}{(1-D)t} \\ \frac{dV_{DC}}{(1-D)t} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{buck}} & -\frac{1}{R_{buck}C_{buck}} \end{bmatrix} \begin{bmatrix} I_L \\ V_{DC} \end{bmatrix} \rightarrow \frac{dX}{(1-D)t} = [A_2][X] \tag{4-10}$$

where V_{SO} defines the DC input voltage source, V_{DC} defines the total DC-link voltage, I_C, I_{DC}, and I_L is the DC current flowing through the filter capacitor C_{buck}, resistor R_{buck}, and inductor L_{buck}, respectively.

By equating (4-9) and (4-10), the periodic state-space equation over the switching period t is given by:

$$\frac{dX}{dt} = [A_1]X + [B_1 D]U \tag{4-11}$$

where D is the duty cycle, $U = V_{SO}$ presents the vector of DC input source, R_{buck} is the buck converter's load resistor, $X = \begin{bmatrix} I_L \\ V_{DC} \end{bmatrix}$ defines the vector of state variables, and

$A_1 = \begin{bmatrix} 0 & -\frac{1}{L_{buck}} \\ \frac{1}{C_{buck}} & -\frac{1}{R_{buck}C_{buck}} \end{bmatrix}$ and $B_1 = \begin{bmatrix} \frac{1}{L_{buck}} \\ 0 \end{bmatrix}$ defines the buck converter system dynamics.

From (4-11), the behaviour for small deviations of *D*, *U*, and *X* from an operating point is considered as given by:

$$X => X_O + x,\ D => D_O + d,\ U => U_O + u \tag{4-12}$$

where the X_O, D_O, and U_O define the steady-state operating point while *x*, *d*, and *u* are the small perturbations from the operating point.

By substituting (4-12) into (4-11), one can obtain:

$$\frac{dX_O}{dt} + \frac{dx}{dt} = [A_1][X_O + x] + [B_1][D_O U_O + D_O u + dU_O + du] \tag{4-13}$$

From (4-13), X_O and $D_O U_O$ are ignored since those are defined to be the steady-state point. The same approach is considered for the perturbation terms as the product of *d and u* is very small. This yields the final linear time-invariant state-space averaged equation as follows:

$$\frac{dx}{dt} = [A_1][x] + [B_1][D_O u + dU_O] \tag{4-14}$$

$$\frac{di_L}{dt} = -\frac{v_{DC}}{L_{buck}} + \frac{D_O v_{SO} + dV_{SO}}{L_{buck}} \tag{4-15}$$

$$\frac{dv_{DC}}{dt} = \frac{i_L}{C_{buck}} - \frac{v_{DC}}{R_{buck}C_{buck}} \tag{4-16}$$

By taking Laplace transform,

$$si_L(s) = -\frac{v_{DC}(s)}{L_{buck}} + \frac{D_O(s)v_{SO}(s) + d(s)V_{SO}(s)}{L_{buck}} \quad \rightarrow$$
$$sL_{buck}i_L(s) = -v_{DC}(s) + D_O(s)v_{SO}(s) + d(s)V_{SO}(s) \tag{4-17}$$

$$sv_{DC}(s)C_{buck} = i_L(s) - \frac{v_{DC}(s)}{R_{buck}} \rightarrow i_L(s) = sv_{DC}(s)C_{buck} + \frac{v_{DC}(s)}{R_{buck}} \tag{4-18}$$

A linear DC output voltage $v_{DC}(s)$ equation in (4-20) is formed by equating (4-17) and (4-18) as follows:

$$sL_{buck}\left(sv_{DC}(s)C_{buck}+\frac{v_{DC}(s)}{R_{buck}}\right)=-v_{DC}(s)+D_O(s)v_{SO}(s)+d(s)V_{SO}(s)\rightarrow$$

$$v_{DC}(s)\left(1+s\frac{L_{buck}}{R_{buck}}+s^2L_{buck}C_{buck}\right)=D_O(s)v_{SO}(s)+d(s)V_{SO}(s)\qquad\rightarrow \tag{4-19}$$

$$v_{DC}(s)=\frac{D_O(s)v_{SO}(s)+d(s)V_{SO}(s)}{s^2L_{buck}C_{buck}+s\frac{L_{buck}}{R_{buck}}+1}$$

$$v_{DC}(s)=\left(D_O(s)\frac{v_{SO}(s)}{V_{SO}(s)}+d(s)\right)\left(\frac{V_{SO}(s)}{s^2L_{buck}C_{buck}+s\frac{L_{buck}}{R_{buck}}+1}\right) \tag{4-20}$$

where the first bracket defines the buck converter's input voltage deviation at the operating point and the second bracket defines the buck converter's transfer function $G_{conv}(s)$ for designing the voltage closed loop controller $G_v(s)$.

Hence, the control system of the DC-DC buck converter can be simply illustrated by the single-line block diagram of Figure 4-5 below.

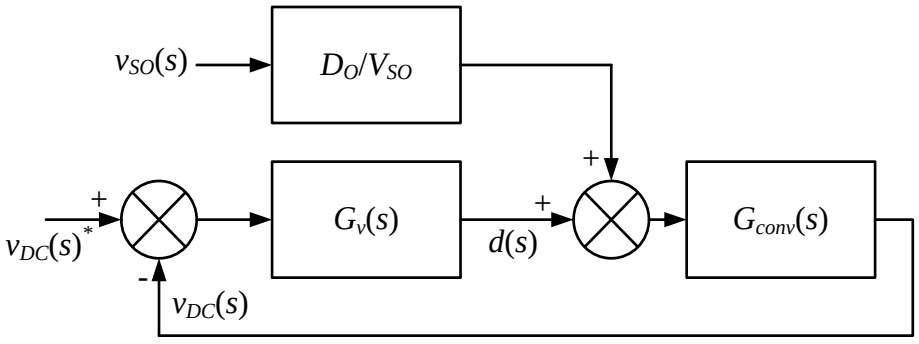

Figure 4-5. Block diagram of the buck converter with voltage loop feedback control.

As for P, PI, and PID controllers, the $G_v(s)$ shown in Figure 4-5 is basically an error amplifier for the voltage mode closed loop controller to generate the duty cycle demand d for the switching device of the buck converter. From [187], the transfer function of $G_v(s)$ is defined as:

$$G_v(s) = \frac{A}{s}\left[\frac{1+\frac{s}{\omega_{z\_buck}}}{1+\frac{s}{\omega_{p\_buck}}}\right] \tag{4-21}$$

where A is the gain of the error amplifier, ω_{z_buck} (i.e., ω_{cross_buck}/K) and ω_{p_buck} (i.e., $\omega_{cross\_buck} \times K$), respectively, are the zero- and pole-frequency based on the selected crossover frequency ω_{cross_buck} and K factor value [187].

Appendix F and Appendix G show the real-time implementation of the buck converter and its associated voltage loop feedback control which is represented by (4-21), respectively.

4.3.2 DC-DC Boost Converter

Compared with the proposed DC-DC buck converter operating at 2 kHz, the boost type possesses high efficient operation with reduced current ratings and increased the bandwidth of the converter (i.e., 25 kHz); therefore, resulting in smaller size of $L_{boost}C_{boost}$ output filter. Thus, it has also been chosen to provide variable DC voltage-levels for each H-bridge inverter in accordance to the resultant modulation index m_i.

Similarly, the voltage closed loop controller of the DC-DC boost converter is designed in CCM using the state-space averaging modelling technique with Venable approach [187]. From Figure 4-1(b), by considering the small deviation and the steady-state operating point of the boost converter, the state-space equation for mode 1 (i.e., switch is on) and mode 2 (i.e., switch is off) are defined in (4-22) and (4-23), respectively.

$$\begin{bmatrix}\frac{dI_L}{DT}\\ \frac{dV_{DC}}{DT}\end{bmatrix} = \begin{bmatrix}0 & 0\\ 0 & -\frac{1}{R_{boost}C_{boost}}\end{bmatrix}\begin{bmatrix}I_L\\ V_{DC}\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}V_{SO} \rightarrow \frac{dX}{Dt} = [A_1][X] + [B_1]U \tag{4-22}$$

$$\begin{bmatrix}\frac{dI_L}{(1-D)T}\\ \frac{dV_{DC}}{(1-D)T}\end{bmatrix} = \begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C_{boost}} & -\frac{1}{R_{boost}C_{boost}}\end{bmatrix}\begin{bmatrix}I_L\\ V_{DC}\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}V_{SO} \rightarrow \frac{dX}{(1-D)t} = [A_2][X] + [B_2]U \tag{4-23}$$

where V_{SO} defines the DC input voltage source, V_{DC} defines the total DC-link voltage, I_C, I_{DC}, and I_L is the DC current flowing through the filter capacitor C_{boost}, resistor R_{boost}, and inductor L_{boost}, respectively.

By equating (4-22) and (4-23), the periodic state-space equation over the switching period t is given by:

$$\frac{dX}{dt} = \left[A_1 D + A_2 (1-D)\right] X + \left[B_1\right] U \tag{4-24}$$

where $X = \begin{bmatrix} I_L \\ V_{DC} \end{bmatrix}$ defines the vector of state variables, $A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_{boost} C_{boost}} \end{bmatrix}$, $A_2 = \begin{bmatrix} 0 & -\frac{1}{L_{boost}} \\ \frac{1}{C_{boost}} & -\frac{1}{R_{boost} C_{boost}} \end{bmatrix}$, and $B_1 = \begin{bmatrix} \frac{1}{L_{boost}} \\ 0 \end{bmatrix}$ defines the boost converter system dynamics, D is the duty cycle, $U = V_{SO}$ presents the vector of DC input source, and R_{boost} is the boost converter's load resistor.

From (4-24), the behaviour for small deviations of D, U, and X from an operating point is considered as given by:

$$X => X_O + x,\ D => D_O + d\ ,\ U => U_O + u \tag{4-25}$$

where the X_O, D_O, and U_O define the steady-state operating point while x, d, and u are the small perturbations from the operating point.

By substituting (4-25) into (4-24), one can obtain:

$$\begin{aligned} &\frac{dX_O}{dt} + \frac{dx}{dt} = \left[\left(A_1 D_o + A_2 (1-D_o)\right) + (A_1 - A_2) d\right]\left[X_O + x\right] + \left[B_1\right]\left[U_O + u\right] \quad \rightarrow \\ &\frac{dX_O}{dt} + \frac{dx}{dt} = \left[A_1 D_o + A_2 (1-D_o)\right]\left[X_O + x\right] + \left[(A_1 - A_2) d\right]\left[X_O + x\right] + \left[B_1\right]\left[U_O + u\right] \end{aligned} \tag{4-26}$$

From (4-26), X_O, $D_O X_O$, and U_O are ignored since those are defined to be the steady-state point. The same approach is considered for the perturbation terms as the product of *d and x* is very small. This yields the final linear time-invariant state-space averaged equation as follows:

$$\frac{dx}{dt}=\left[A_1D_o+A_2\left(1-D_o\right)\right]\left[x\right]+\left[\left(A_1-A_2\right)d\right]\left[X_O\right]+\left[B_1\right]\left[u\right] \tag{4-27}$$

$$\frac{di_L}{dt}=-\frac{(1-D_O)v_{DC}}{L_{boost}}+\frac{dV_{DC}}{L_{boost}}+\frac{v_{SO}}{L_{boost}} \tag{4-28}$$

$$\frac{dv_{DC}}{dt}=\frac{(1-D_O)i_L}{C_{boost}}-\frac{v_{DC}}{R_{boost}C_{boost}}-\frac{dI_L}{C_{boost}} \tag{4-29}$$

By taking Laplace transform,

$$\begin{aligned} si_L(s)&=-\frac{(1-D_O(s))v_{DC}(s)}{L_{boost}}+\frac{d(s)V_{DC}(s)}{L_{boost}}+\frac{v_{SO}(s)}{L_{boost}} \quad \rightarrow \\ i_L(s)&=-\frac{(1-D_O(s))v_{DC}(s)}{sL_{boost}}+\frac{d(s)V_{DC}(s)}{sL_{boost}}+\frac{v_{SO}(s)}{sL_{boost}} \end{aligned} \tag{4-30}$$

$$sv_{DC}(s)=\frac{(1-D_O(s))i_L(s)}{C_{boost}}-\frac{v_{DC}(s)}{R_{boost}C_{boost}}-\frac{d(s)I_L(s)}{C_{boost}} \tag{4-31}$$

A linear DC output voltage $v_{DC}(s)$ equation in (4-33) is formed by equating (4-30) and (4-31) as follows.

$$sv_{DC}(s)=\left(\frac{1-D_O(s)}{C_{boost}}\right)\left(-\frac{(1-D_O(s))v_{DC}(s)}{sL_{boost}}+\frac{d(s)V_{DC}(s)}{sL_{boost}}+\frac{v_{SO}(s)}{sL_{boost}}\right)-\frac{v_{DC}(s)}{R_{boost}C_{boost}}-\frac{d(s)I_L(s)}{C_{boost}} \rightarrow$$

$$sv_{DC}(s)=\left(-\frac{(1-D_O(s))^2v_{DC}(s)}{sL_{boost}C_{boost}}+\frac{(1-D_O(s))d(s)V_{DC}(s)}{sL_{boost}C_{boost}}+\frac{(1-D_O(s))v_{SO}(s)}{sL_{boost}C_{boost}}\right)-\frac{v_{DC}(s)}{R_{boost}C_{boost}}-\frac{d(s)I_L(s)}{C_{boost}} \rightarrow$$

$$sv_{DC}(s)+\frac{v_{DC}(s)}{R_{boost}C_{boost}}+\frac{(1-D_O(s))^2v_{DC}(s)}{sL_{boost}C_{boost}}=\frac{(1-D_O(s))d(s)V_{DC}(s)}{sL_{boost}C_{boost}}+\frac{(1-D_O(s))v_{SO}(s)}{sL_{boost}C_{boost}}-\frac{d(s)I_L(s)}{C_{boost}} \rightarrow$$

$$s^2L_{boost}C_{boost}v_{DC}(s)+\frac{sL_{boost}v_{DC}(s)}{R_{boost}}+(1-D_O(s))^2v_{DC}(s)=(1-D_O(s))d(s)V_{DC}(s) \rightarrow$$
$$+(1-D_O(s))v_{SO}(s)-sL_{boost}d(s)I_L(s)$$

$$v_{DC}(s)\left(\frac{s^2L_{boost}C_{boost}}{(1-D_O(s))^2}+\frac{sL_{boost}}{(1-D_O(s))^2R_{boost}}+1\right)=\frac{d(s)V_{DC}(s)}{1-D_O(s)}+\frac{v_{SO}(s)}{1-D_O(s)}-\frac{sL_{boost}d(s)I_L(s)}{(1-D_O(s))^2} \rightarrow$$

$$v_{DC}(s)\left(\frac{s^2L_{boost}C_{boost}}{(1-D_O(s))^2}+\frac{sL_{boost}}{(1-D_O(s))^2R_{boost}}+1\right)=\frac{d(s)\dfrac{V_{SO}(s)}{(1-D_O(s))}}{1-D_O(s)}+\frac{v_{SO}(s)}{1-D_O(s)} \rightarrow$$
$$-sL_{boost}d(s)\frac{V_{SO}(s)}{(1-D_O(s))^4R_{boost}}$$

$$v_{DC}(s)\left(\frac{s^2L_{boost}C_{boost}}{(1-D_O(s))^2}+\frac{sL_{boost}}{(1-D_O(s))^2R_{boost}}+1\right)=\frac{v_{SO}(s)}{1-D_O(s)}+\frac{d(s)V_{SO}(s)}{(1-D_O(s))^2}\left(1-\frac{sL_{boost}}{(1-D_O(s))^2R_{boost}}\right) \rightarrow$$

$$v_{DC}(s)=\frac{\dfrac{v_{SO}(s)}{1-D_O(s)}+\dfrac{d(s)V_{SO}(s)}{(1-D_O(s))^2}\left(1-\dfrac{sL_{boost}}{(1-D_O(s))^2R_{boost}}\right)}{\dfrac{s^2L_{boost}C_{boost}}{(1-D_O(s))^2}+\dfrac{sL_{boost}}{(1-D_O(s))^2R_{boost}}+1} \tag{4-32}$$

$$v_{DC}(s)=\left(\frac{\dfrac{(1-D_O(s))v_{SO}(s)}{V_{SO}(s)}}{1-\dfrac{sL_{boost}}{(1-D_O(s))^2R_{boost}}}+d(s)\right)\left(\frac{\dfrac{V_{SO}(s)}{(1-D_O(s))^2}\left(1-\dfrac{sL_{boost}}{(1-D_O(s))^2R_{boost}}\right)}{\dfrac{s^2L_{boost}C_{boost}}{(1-D_O(s))^2}+\dfrac{sL_{boost}}{(1-D_O(s))^2R_{boost}}+1}\right) \tag{4-33}$$

where the first bracket defines the boost converter's input voltage deviation at the operating point and the second bracket defines the boost converter's transfer function $G_{conv}(s)$ for designing the voltage closed loop controller $G_v(s)$.

From (4-33), the right-half plane zero (i.e., second bracket) is related to the effective value of the filter inductance L_{boost} and the load resistance R_{boost}. To mitigate the instability effect caused by the right-half plane zero, higher operating switching frequency f_{sw_boost} must be selected to reduce the size of filter inductance L_{boost}; therefore, optimizing the voltage loop performance with a proper selection of the crossover frequency for better transient response.

The control system of the DC-DC boost converter can be simply illustrated by the single-line block diagram of Figure 4-6 below.

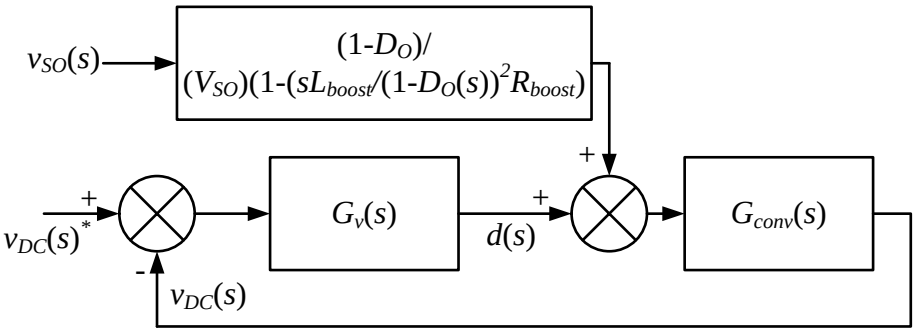

Figure 4-6. Block diagram of the boost converter with voltage loop feedback control.

From Figure 4-6, the transfer function of the error amplifier $G_v(s)$, which generates the duty cycle demand d for the switching device of the boost

converter, is defined as [187]:

$$G_v(s) = \frac{A}{s}\left[\frac{1+\dfrac{s}{\omega_{z\_boost}}}{1+\dfrac{s}{\omega_{p\_boost}}}\right] \tag{4-34}$$

where A is the gain of the error amplifier, ω_{z_boost} (i.e., ω_{cross_boost}/K) and ω_{p_buck} (i.e., $\omega_{cross\_boost} \times K$), respectively, are the zero- and pole-frequency based on the selected crossover frequency ω_{cross_boost} and K factor value [187].

Appendix J and Appendix K show the implementation of the boost converter and its associated voltage loop feedback control model using Matlab/Simulink which is represented by (4-34), respectively.

4.4 Results and Discussion

Similarly, the proposed MSHE-PWM method based single-phase STATCOM system is first studied through various simulation examples using Matlab/Simulink software package [188]. To verify the simulation and theoretical work presented in this chapter, the single-phase five-level CHI presented in Chapter 3 has been scaled-down and analysed. Selected results are chosen to demonstrate the validity of the proposed MSHE-PWM method based STATCOM system. The next subsections present the comparison between the proposed method and the conventional IPD CB-PWM operated with an equivalent frequency (i.e., 1.6 kHz) to show the superiority and effectiveness of the former.

4.4.1 Comparison of MSHE-PWM with distribution ratio of N_1/N_2 = 3/5 against IPD CB-PWM technique

4.4.1.1 Simulation Results

The simulation study of the proposed STATCOM system with separated DC-DC buck converters (see model in Appendix I) is carried out with the system parameters tabulated in Table 4-2.

Table 4-2. System Parameters Used in the Simulation Study.

Buck converter steady-state parameters:
DC voltage source: V_{so} = 240 V Switching frequency: f_{sw_buck} = 2 kHz Filter inductor: L_{buck} = 500 µH Filter capacitor: C_{buck} = 250 µF Filter resistor: R_{buck} = 1 Ω Crossover frequency: ω_{cross_buck} = 5657 rad/s Gain of error amplifier: A = 36.66 Zero-frequency: ω_{z_buck} = 752.24 rad/s Pole-frequency: ω_{p_buck} = 742539.51 rad/s
Single-phase power system parameters:
S_{base} = 1.44 kVA, V_{base} = 240 V_{rms}, I_{base} = 6 A_{rms}, Z_{base} = 40 Ω Fundamental frequency: f = 50 Hz Single phase power rating = 1 p.u. Single phase grid voltage: v_{pcc} = 1 p.u. Grid resistor: R_s = 0.4 Ω = 0.01 p.u. Grid inductor: L_s = 12.7 mH Grid impedance: Z_s = 4 Ω = 0.1 p.u. Coupling resistor: R_f = 4 Ω = 0.1 p.u. Coupling inductor: L_f = 127 mH Coupling impedance: Z_f = 40 Ω = 1 p.u. Load A R_l: S_{l_A} = P_{l_A} = 960 W = 0.67 p.u. Load A current: i_{l_A} = 4 A_{rms} = 0.67 p.u. Load B R_lL_l: S_{l_B} = 1360 W = 0.94 p.u., P_{l_B} = 960 W = 0.67 p.u., Q_{l_B} = 960 VAR = 0.67 p.u. Load B current: i_{l_B} = 5.64 A_{rms} = 0.94 p.u. d-axis Proportional gain: K_{p_id} = 0.21 q-axis Proportional gain: K_{p_iq} = 1.63

The performance of the STATCOM system's dynamics, steady-state, and transient characteristics are investigated at different loading conditions using a linear single-phase reactive load that changes from resistive load A to inductive load B (i.e., from unity to lagging PF) at the time of 1 second.

The implementation of the proposed line-to-neutral MSHE-PWM voltage waveform produced by the STATCOM system and its associated spectrum for load B is illustrated in Figure 4-7.

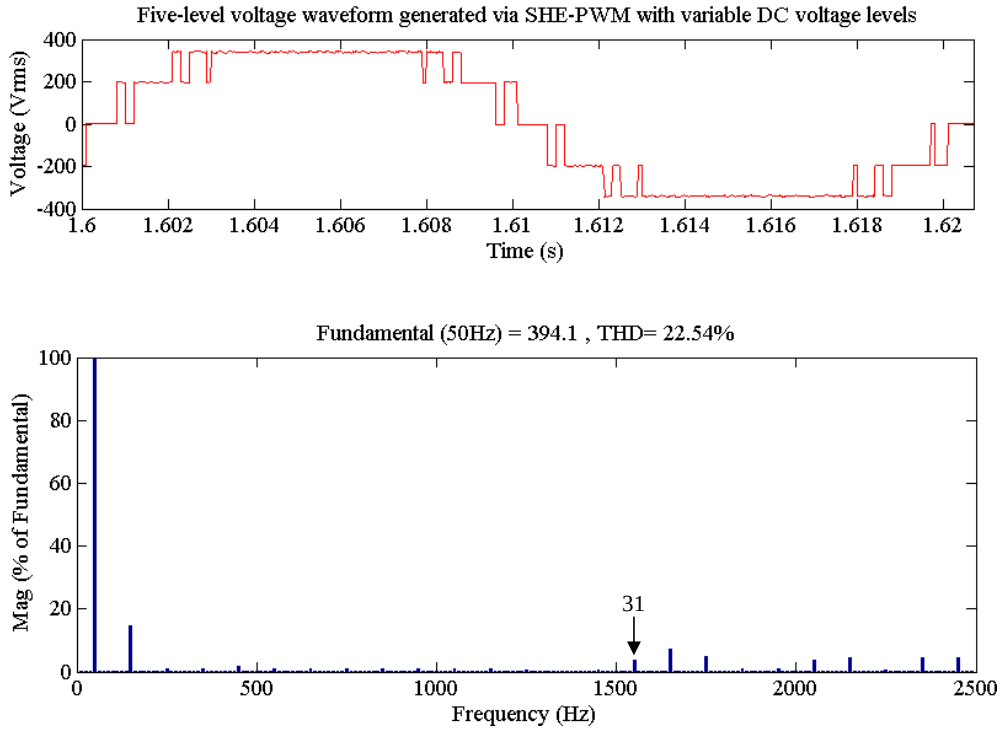

Figure 4-7. Simulation results of Case I (i.e., N_1/N_2 = 3/5) of single-phase (i.e., line-to-neutral) five-level SHE-PWM output voltage waveform and its spectrum for load B.

It is observed that the intended low-order non-triplen harmonics (i.e., 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, and 29^{th}) which were meant to be eliminated are absent and the next harmonic appears in the line-to-neutral spectrum is the 31^{st}. From Figure 4-7, it is worth noting that the proposed MSHE-PWM method implemented with only eight switching angles per quarter cycle (i.e., 32 switching angles per one cycle) makes the effective switching frequency of the inverter equals to 1.6 kHz (i.e., 32 $\times$50 Hz).

Figure 4-8 illustrates the dynamic and transient responses of the MSHE-PWM based STATCOM system controlled by the proposed control scheme under different loading conditions (i.e., from resistive load A to inductive load B). Specifically, Figure 4-8(e) illustrates the grid voltage sag (i.e., reduced by about 7% from the nominal voltage value), which is caused by the voltage drop across the grid impedance Z_s, when the load is changed from A to B at the time of 1 second. This voltage sag is then restored back to a unity by the proposed STATCOM system via reactive current compensation.

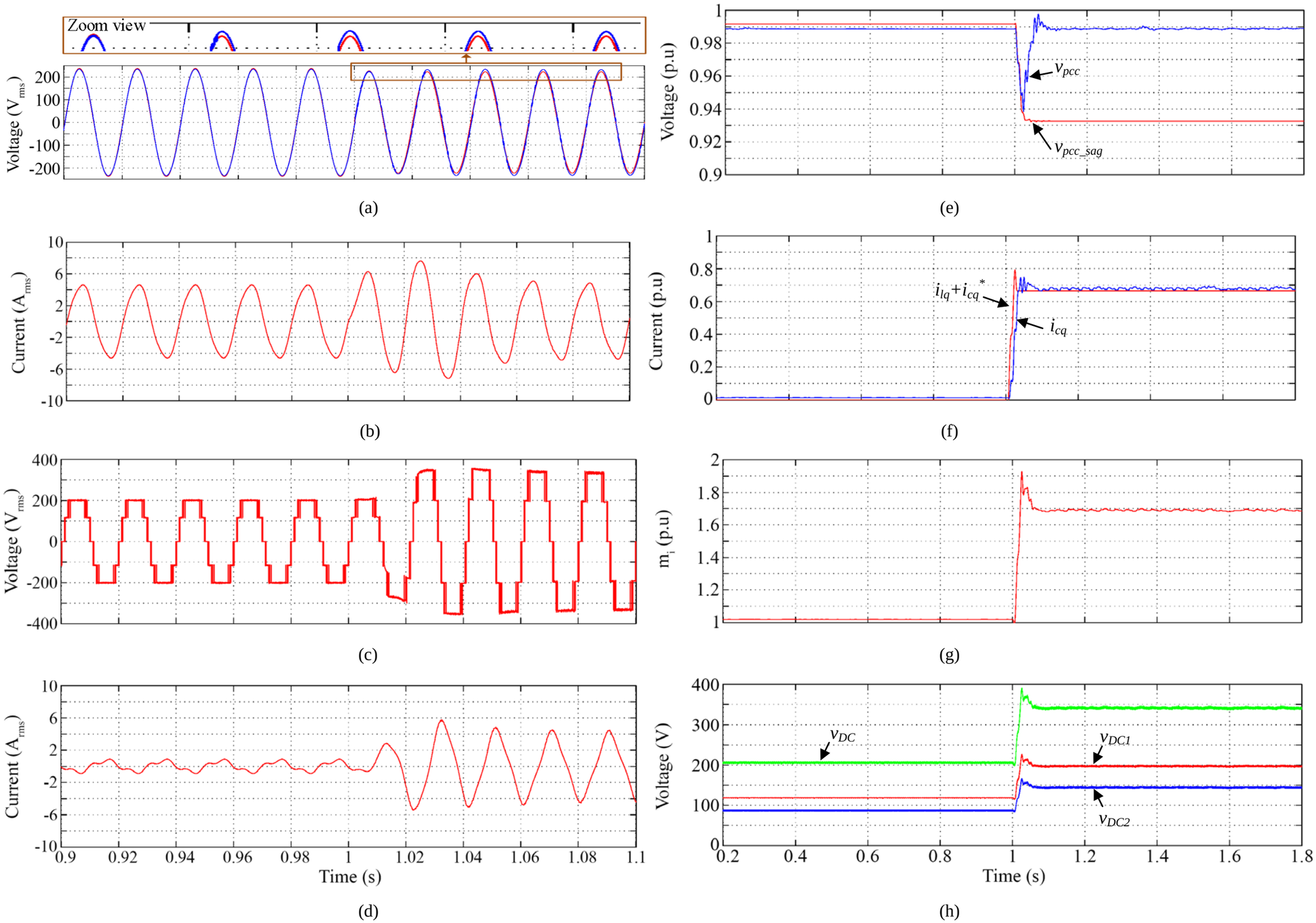

Figure 4-8. Simulation results of AC single-phase line-to-neutral (a) grid voltage v_{pcc}, (b) grid current i_s, (c) STATCOM voltage v_c, (d) STATCOM current i_c, and DC quantities of (e) grid voltage magnitude v_{pcc}, (f) ramp change of measured i_{cq} and reactive current references $i_{lq} + i_{cq}^{*}$, (g) modulation indexes m_i, and (h) buck converters output voltages v_{DC1} and v_{DC2} at different loading conditions.

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Figure 4-8(f) shows the characteristic of the STATCOM reactive current i_{cq} which is consistently tracking the ramp-change of the reactive current references $i_{lq} + i_{cq}^{*}$. Similar observation is also seen from Figure 4-8(h), where the characteristic of each DC output voltage (i.e., v_{DC1} and v_{DC2}) generated by the buck converters in response to the resultant modulation index m_i (see Figure 4-8(g)) provided by the proposed control scheme is demonstrated.

To further show the effectiveness of the proposed MSHE-PWM method in producing a high quality output voltage waveform, the same STATCOM system is operated and compared to the conventional IPD CB-PWM with an equivalent switching frequency of 1.6 kHz (see model in Appendix H).

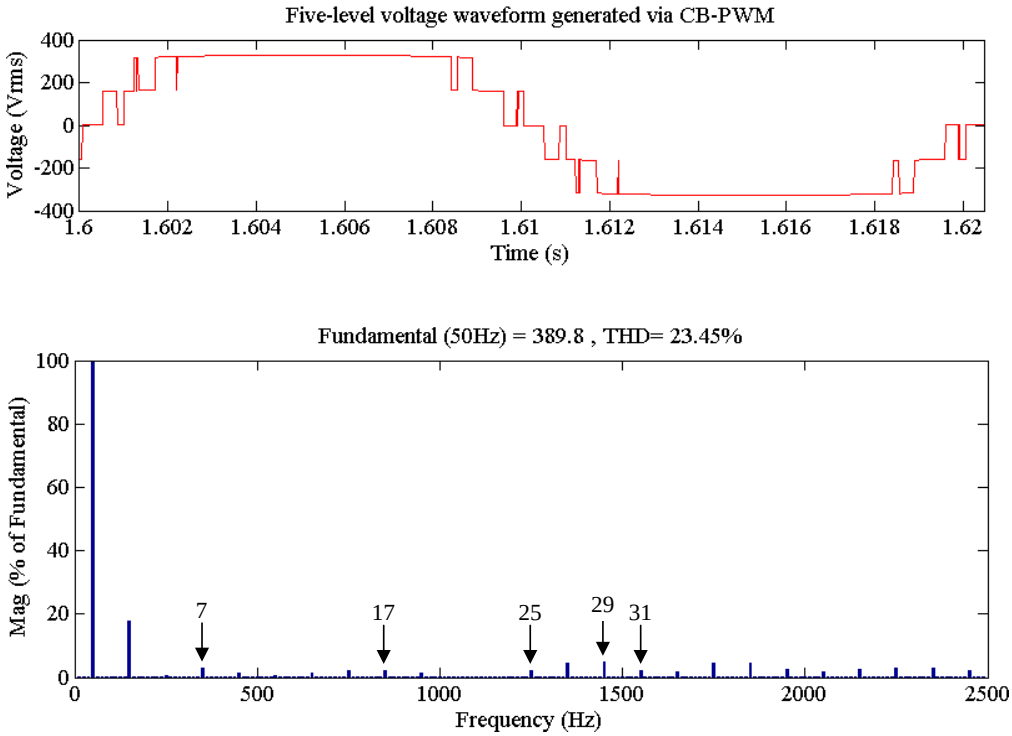
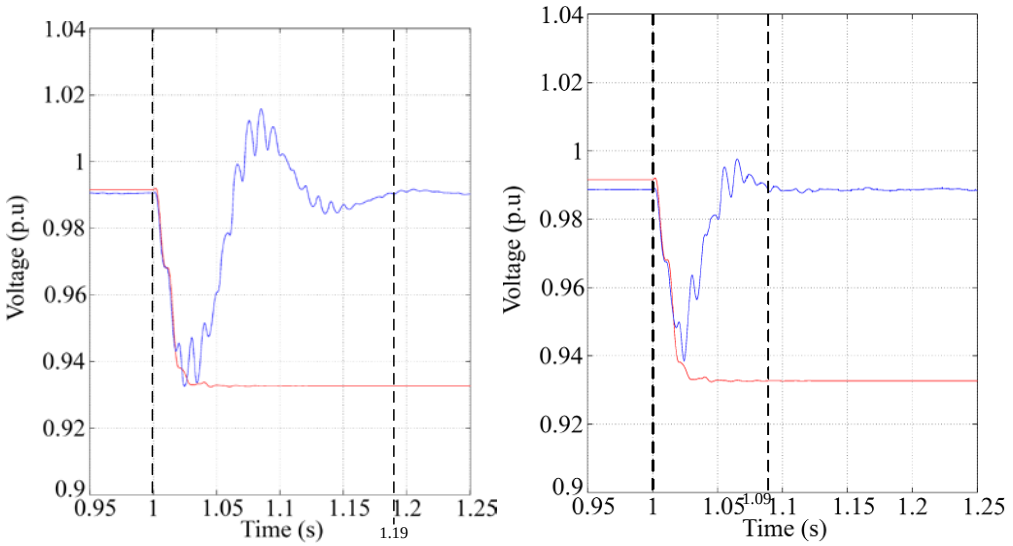


Figure 4-9. Simulation results of single-phase (i.e., line-to-neutral) five-level CB-PWM output voltage waveform and its spectrum for load B.

As the inverter is driven into the overmodulation region (i.e., $m_i > 1$ p.u.) for the given loading condition (i.e., capacitive mode), low-order harmonics start to appear in the case of CB-PWM due to the pulse drop which is observed from Figure 4-9. A quick comparison with the spectrum presented in Figure 4-7 that is offered by the proposed MSHE-PWM with variable DC voltage-levels technique, reveals that the harmonics are tightly controlled even in the

case when the inverter operates in overmodulation region; therefore, offering considerably lower THD and wider inverter's bandwidth with low-switching frequency, hence, less switching losses and cooling requirements.

For completeness, the dynamic and transient performances of the proposed MSHE-PWM method and the conventional CB-PWM technique employing with the same proposed control scheme are also investigated as shown in Figure 4-10. Specifically, Figure 4-10(b) demonstrates the performance of the MSHE-PWM based STATCOM, which took approximately 4 cycles to detect and restore the grid voltage v_{pcc} back to a unity and then reached steady-state. This gives about 50% response time improvement of the system [98] when compared to the conventional CB-PWM based STATCOM with separated DC-link voltage sources (see Figure 4-10(a)).



(a) (b)

Figure 4-10. Simulation results of restoring the grid voltage v_{pcc} sags using (a) an equivalent CB-PWM and (b) proposed MSHE-PWM technique.

4.4.1.2 Experiment Results

A scaled-down laboratory prototype based on the single-phase STATCOM system as shown in Chapter 3 under Section 3.4.2 has been developed and tested to validate the theoretical and the simulation findings. Since the purpose of this chapter is to explore the advantages of the new MSHE-PWM, hence for convenience, a five-level CHI with separated DC

voltage sources (see Figure 4-11) forms the heart of the proposed STATCOM system which is studied with the system parameters of Table 4-3.

Table 4-3. System Parameters Used in the Experimental Work.

Single-phase power system parameters:
S_{base} = 90 VA, V_{base} = 60 V_{rms}, I_{base} = 1.5 A_{rms}, Z_{base} = 40 Ω
Fundamental frequency: f = 50 Hz Single phase power rating = 1 p.u. Single phase grid voltage: v_{pcc} = 1 p.u. Coupling resistor: R_f = 4 Ω = 0.1 p.u. Coupling inductor: L_f = 127 mH Coupling impedance: Z_f = 40 Ω = 1 p.u. Load A R_l: S_{l_A} = P_{l_A} = 60 W = 0.67 p.u. Load A current: i_{l_A} = 1 A_{rms} = 0.67 p.u. Load B R_lL_l: S_{l_B} = 85 W = 0.94 p.u., P_{l_B} = 60 W = 0.67 p.u., Q_{l_B} = 60 VAR = 0.67 p.u. Load B current: i_{l_B} = 1.4 A_{rms} = 0.94 p.u.

From Table 4-3, the coupling impedance Z_f is obtained based on the rated grid voltage v_{pcc} (i.e., 60 V_{rms}) and current (i.e., 1.5 A_{rms}). It should be noted that due to the limited number of DC voltage sources, the operating voltage in the experiments has been scaled down from 240 V_{rms} to 60 V_{rms} as compared with the simulation study (i.e., Table 4-2). However, the impedance of load remains the same; therefore, this has no effect on the controller parameters (i.e., the gains of P-controllers) as the operating current is reduced by the same proportional amount. Thus, same controller parameters of the proposed control scheme are employed in both the simulation and experimental work.

The real-time analysis of STATCOM system's dynamic, steady-state, transient response, and harmonics performances are carried out with a 90 W of linear single-phase reactive load that changes from resistive R_l to inductive R_lL_l characteristic (i.e., from unity to lagging PF) at the time of the 3rd second (see Figure 4-12). Specifically, Figure 4-12(a) illustrates the grid voltage sag (i.e., about 4% of the nominal voltage) caused by the voltage drop across the 240 V_{rms} to 60 V_{rms} step-down transformer when only a resistive load (i.e., load A) is connected to the power system (i.e., from 0 to 3 seconds).

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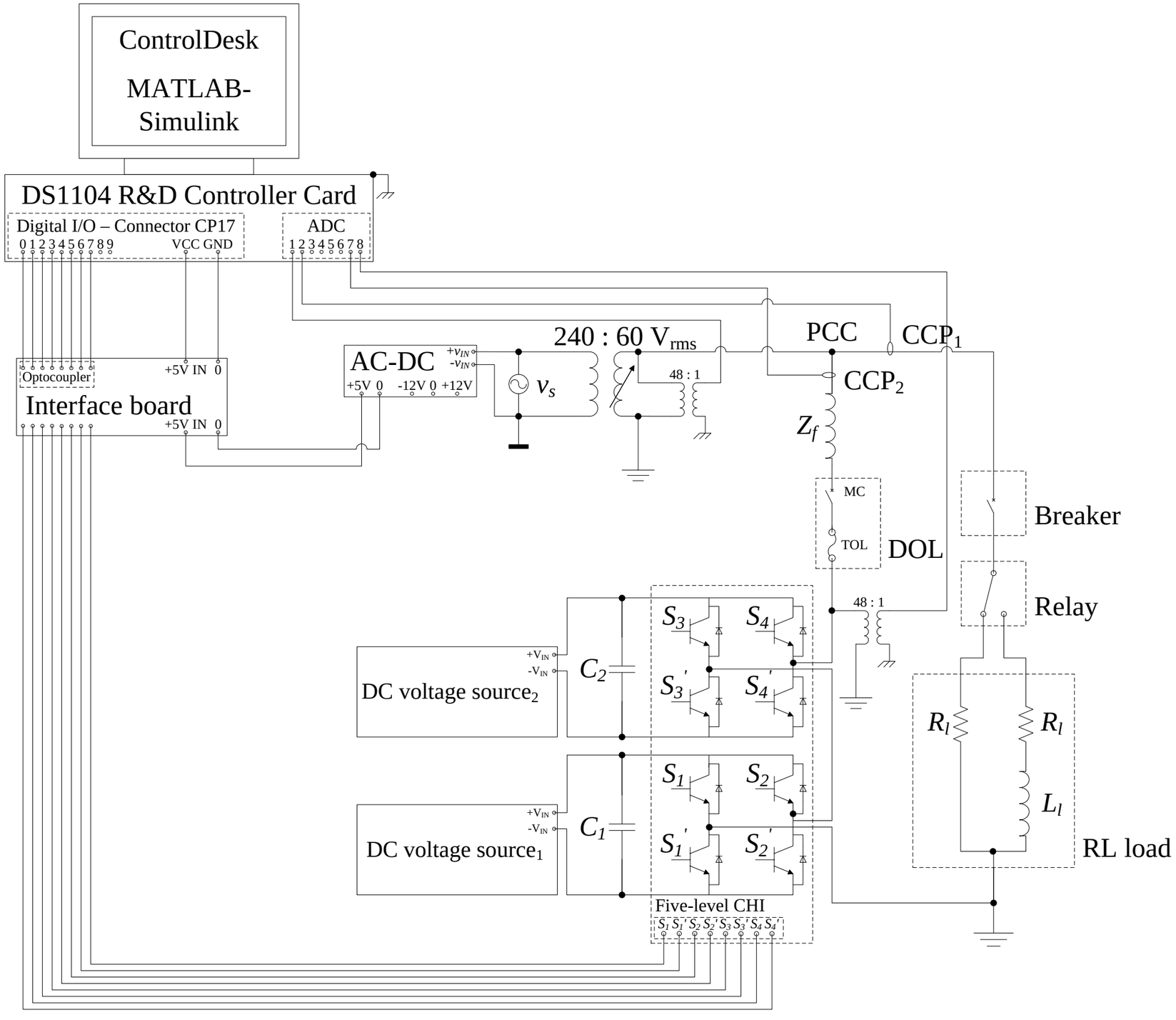
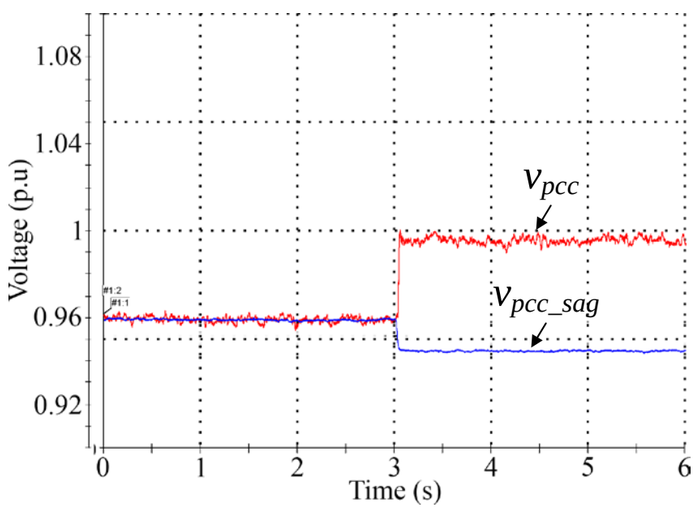
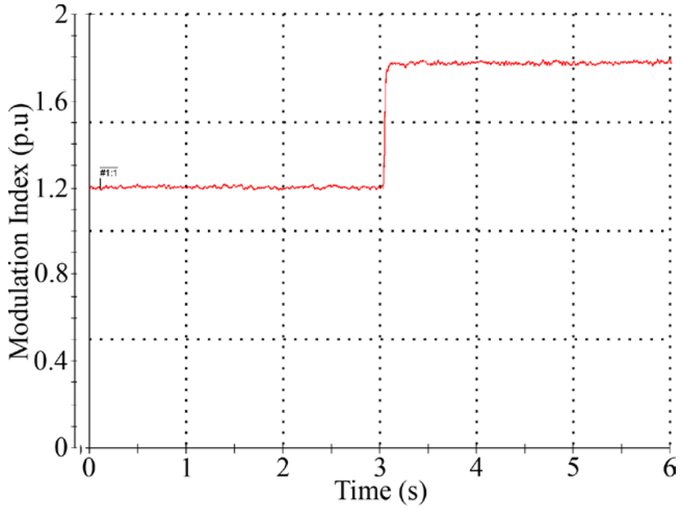


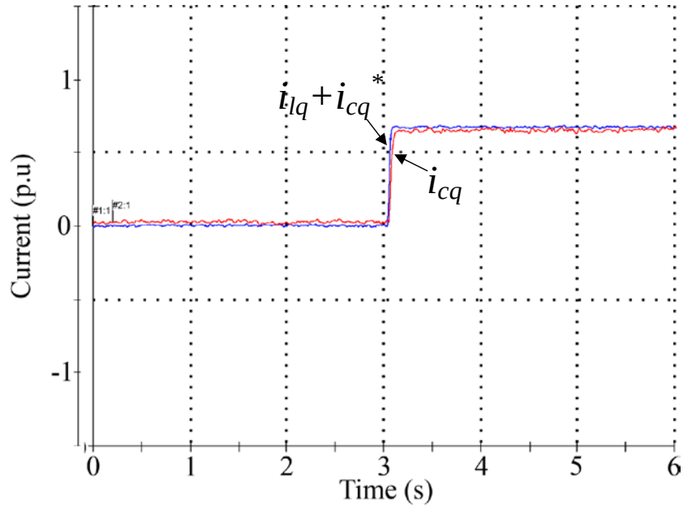
Figure 4-11: Circuit diagram of five-level SHE-PWM (i.e., Case I (i.e., N_1/N_2 = 3/5) H-bridge inverter based single-phase STATCOM with the separated DC voltage sources.



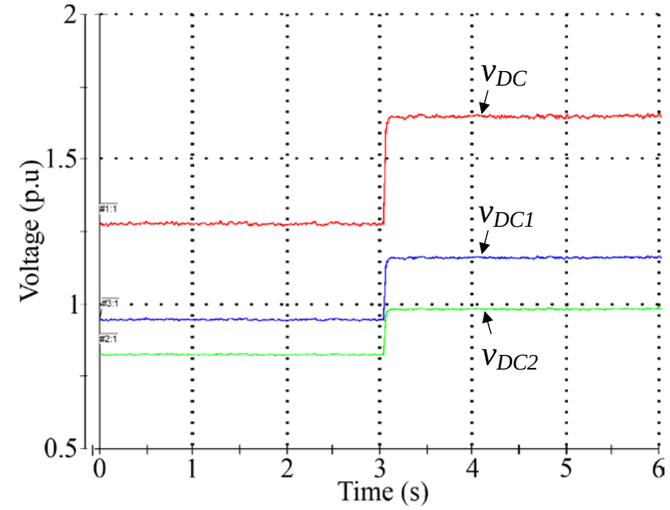
(a)



(c)



(b)

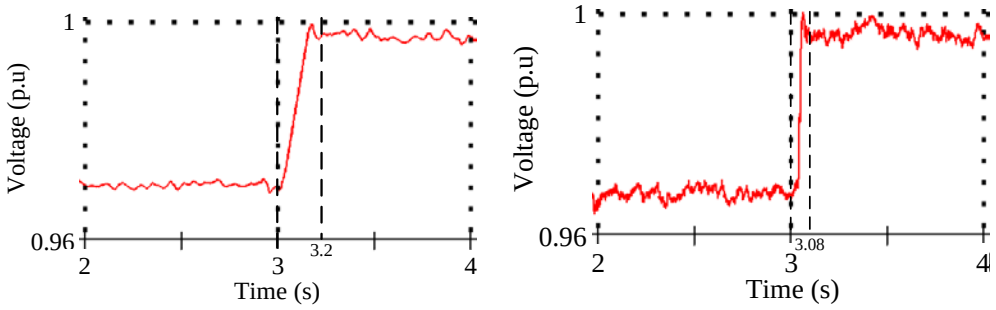


(d)

Figure 4-12. Experimental results of DC vectors in p.u. value (a) grid voltage magnitude v_{pcc}, (b) ramp change of measured i_{cq} and reactive current references $i_{lq} + i_{cq}^{*}$, (c) modulation indexes m_i, and (d) DC voltage-levels v_{DC1} and v_{DC2} at different loading conditions.

Since there is no reactive component being extracted from the load side (i.e., i_{lq} = 0) at this interval, the STATCOM reactive current i_{cq} is zero (see Figure 4-12(b)) and hence there is no VAR exchange between the STATCOM system and the power system at PCC. Nevertheless, at the next interval (i.e., from 3 to 6 seconds), the grid voltage v_{pcc} is successfully restored back to a unity after providing reactive current compensation by the STATCOM system. Figure 4-12(b) further shows the characteristic of the STATCOM reactive current i_{cq} controller which is consistently tracking the ramp-change of reactive current references i_{lq} + i_{cq}^{*} value. On the other hand, Figure 4-12(d) presents the characteristics of the DC voltages in response to the resultant modulation index m_i shown in Figure 4-12(c).

The dynamic and transient performances of the proposed MSHE-PWM method against the conventional IPD CB-PWM technique are also experimentally verified and compared under the same loading conditions (i.e., a step change from load A to load B) as illustrated in Figure 4-13.



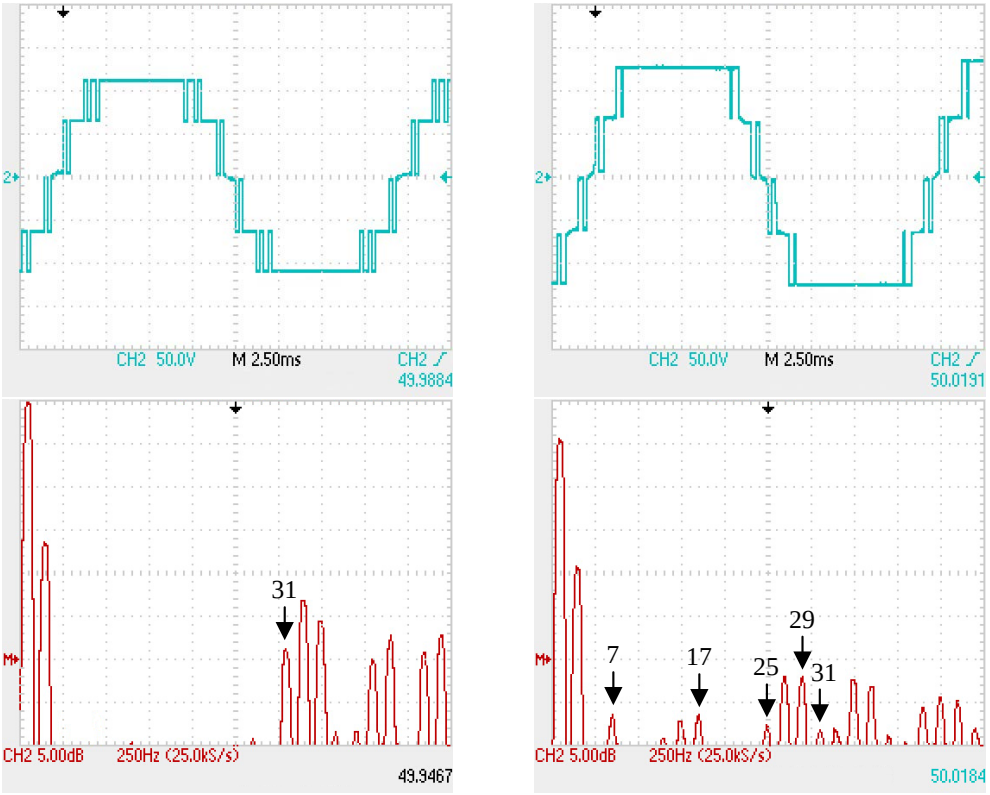
(a) (b)

Figure 4-13. Experimental results of restoring the grid voltage v_{pcc} sags using (a) an equivalent CB-PWM and (b) proposed MSHE-PWM technique.

Although a small deviation between simulation and practical results is always appreciated, nevertheless, it is worth noting that the proposed method takes only half of the time response (i.e., approximately 4 cycles) than the conventional CB-PWM technique to restore the grid voltage v_{pcc} back to unity (see Figure 4-13(b)). This is due to the constant switching transitions/angles of the proposed MSHE-PWM technique being able to increase the inverter bandwith and eliminate maximum number of harmonics with relatively equivalent switching frequency (i.e., 1.6 kHz). Furthermore, the grid voltage

v_{pcc} which is regulated by the MSHE-PWM technique (see Figure 4-13(b)), contains some ripples as opposed to the CB-PWM (see Figure 4-13(a)) due to the fact that the MSHE-PWM operates with a low-switching frequency and the existence of high-order harmonics (non-eliminated). Nevertheless, these harmonics can be always removed easily with a small size filter without compromising the performance of the system [189].

The real-time single-phase five-level voltage waveforms and the associated spectra for both the proposed MSHE-PWM and the conventional CB-PWM techniques are shown in Figure 4-14(a) and Figure 4-14(b), respectively.



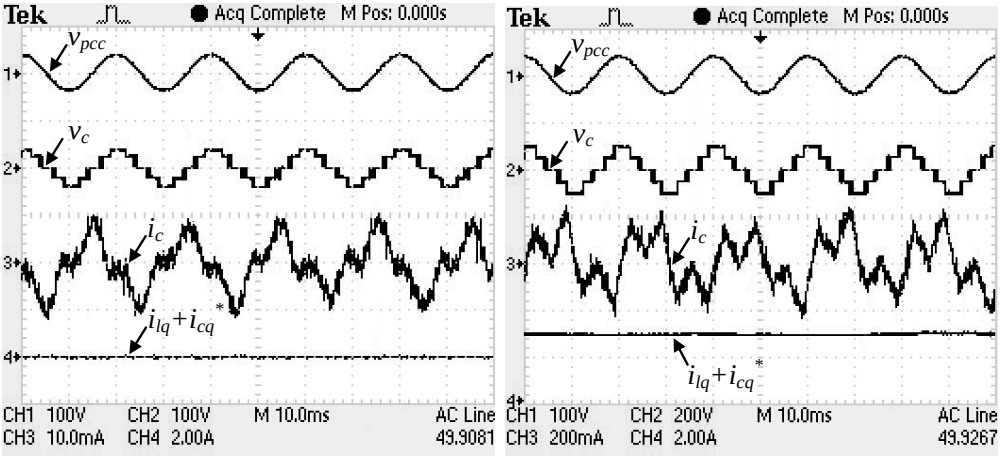
(a) (b)

Figure 4-14. Experimental implementation of line-to-neutral five-level output voltage waveform and the associated spectrum. (a) MSHE-PWM (i.e., N_1/N_2 = 3/5) and (b) CB-PWM technique.

These are in a good match with the simulation results presented in Figure 4-7 and Figure 4-9. Once again, it is confirmed that the proposed MSHE-PWM method offers a tight control of the low-order non-triplen harmonics when

compared to the conventional CB-PWM technique, where low-order harmonics start to appear if the inverter is driven into the overmodulation region. This will necessitate harmonic filtering circuits to be installed in order to attenuate the unwanted harmonic, which in turns increases the construction cost and the size of the system.

Figure 4-15 presents the experimental waveforms of the grid voltage v_{pcc} (i.e., channel 1), the five-level SHE-PWM STATCOM output voltage v_c (i.e., channel 2), the STATCOM output current i_c (i.e., channel 3), and the reactive current references i_{lq} + i_{cq}^* (i.e., channel 4) under different loading conditions.



(a) (b)

Figure 4-15. Experimental results of the proposed MSHE-PWM based single-phase STATCOM in (a) floating mode and (b) capacitive mode operation.

From the channel 3 of Figure 4-15(a) and Figure 4-15(b), the phase distortion in STATCOM current is caused by the 3rd harmonic component (i.e., triplen harmonics) which can be observed from Figure 4-7 and Figure 4-14(a) [190]. Nevertheless, these triplen harmonics are left uncontrolled as they will be eliminated by the 120 electrical degree phase shift characteristic in three-phase system.

The next subsections investigate the performance of the proposed MSHE-PWM based STATCOM system with different distribution ratios (i.e., case I: N_1/N_2 = 3/5 and case II: N_1/N_2 = 3/8).

4.4.2 Comparison of MSHE-PWM with distribution ratio of N_1/N_2 = 3/5 against N_1/N_2 = 3/8.

4.4.2.1 Simulation Results

The simulation study of the proposed STATCOM system with separated DC-DC boost converters (see model in Appendix L) is carried out with the system parameters tabulated in Table 4-4.

Table 4-4. System Parameters Used in the Simulation Study.

Boost converter steady-state parameters:
DC voltage source: V_{so} = 60 V Switching frequency: f_{sw_boost} = 25 kHz Filter inductor: L_{boost} = 6.4 µH Filter capacitor: C_{boost} = 0.3 mF Filter resistor: R_{boost} = 10 Ω Crossover frequency: ω_{cross_boost} = 114 krad/s Gain of error amplifier: A = 3.32 Zero-frequency: ω_{z_boost} = 2224.37 rad/s Pole-frequency: ω_{p_boost} = 58538.43 rad/s
Single-phase power system parameters:
S_{base} = 1.44 kVA, V_{base} = 240 V_{rms}, I_{base} = 6 A_{rms}, Z_{base}= 40 Ω Fundamental frequency: f = 50 Hz Single phase power rating = 1 p.u. Single phase grid voltage: v_{pcc} = 1 p.u. Grid resistor: R_s = 0.4 Ω = 0.01 p.u. Grid inductor: L_s = 12.7 mH Grid impedance: Z_s = 4 Ω = 0.1 p.u. Coupling resistor: R_f = 4 Ω = 0.1 p.u. Coupling inductor: L_f = 127 mH Coupling impedance: Z_f = 40 Ω = 1 p.u. Load A R_lC_l: S_{l_A} = 1360 W = 0.94 p.u., P_{l_A} = 960 W = 0.67 p.u., Q_{l_A} = 960 VAR = 0.67 p.u. Load A current: i_{l_A} = 5.64 A_{rms} = 0.94 p.u. Load B R_lL_l: S_{l_B} = 1360 W = 0.94 p.u., P_{l_B} = 960 W = 0.67 p.u., Q_{l_B} = 960 VAR = 0.67 p.u. Load B current: i_{l_B} = 5.64 A_{rms} = 0.94 p.u. d-axis Proportional gain: K_{p_id} = 0.21 q-axis Proportional gain: K_{p_iq} = 1.63

Similarly, the dynamics, steady-state, and transient characteristics of the STATCOM system are investigated at different loading conditions using a linear single-phase reactive load that changes from resistive load A to inductive load B (i.e., from leading to lagging PF) at the time of 1 second.

The MSHE-PWM waveforms for case II (i.e., N_1/N_2 = 3/8) and the associated spectra are presented in Figure 4-16, where it is clear that all the intended low-order non-triplen harmonics are eliminated and the next harmonic appears in the spectrum would be the 41st. Furthermore, triplen harmonics will be absent between line-to-line voltage.

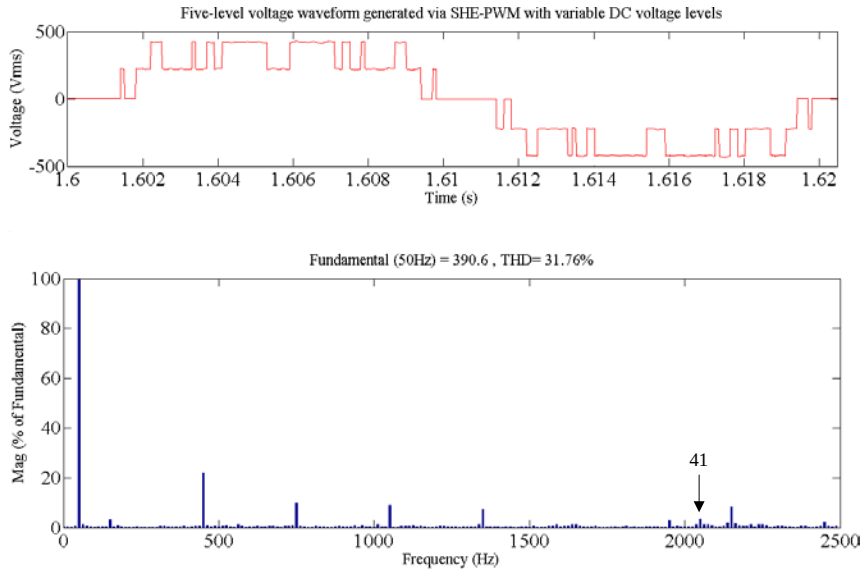


Figure 4-16. Simulation results of Case II (i.e., N_1/N_2 = 3/8) of single-phase (i.e., line-to-neutral) five-level SHE-PWM output voltage waveform and its spectrum for load B.

Figure 4-17 presents the dynamic and transient responses of the MSHE-PWM based STATCOM system (i.e., for Case I) controlled by the proposed control scheme under different loading conditions. Specifically, Figure 4-17(a)-Figure 4-17(d) show the AC line-to-neutral voltages and currents responses for the changes from capacitive load A to inductive load B characteristics. Figure 4-17(e) illustrates the grid voltage swell and sag by about 7% from the nominal voltage value when the load is changed from load A to load B, respectively, at the time of 1 second. These voltage swell and sag are then restored back to a unity by the proposed STATCOM system via reactive current compensation.

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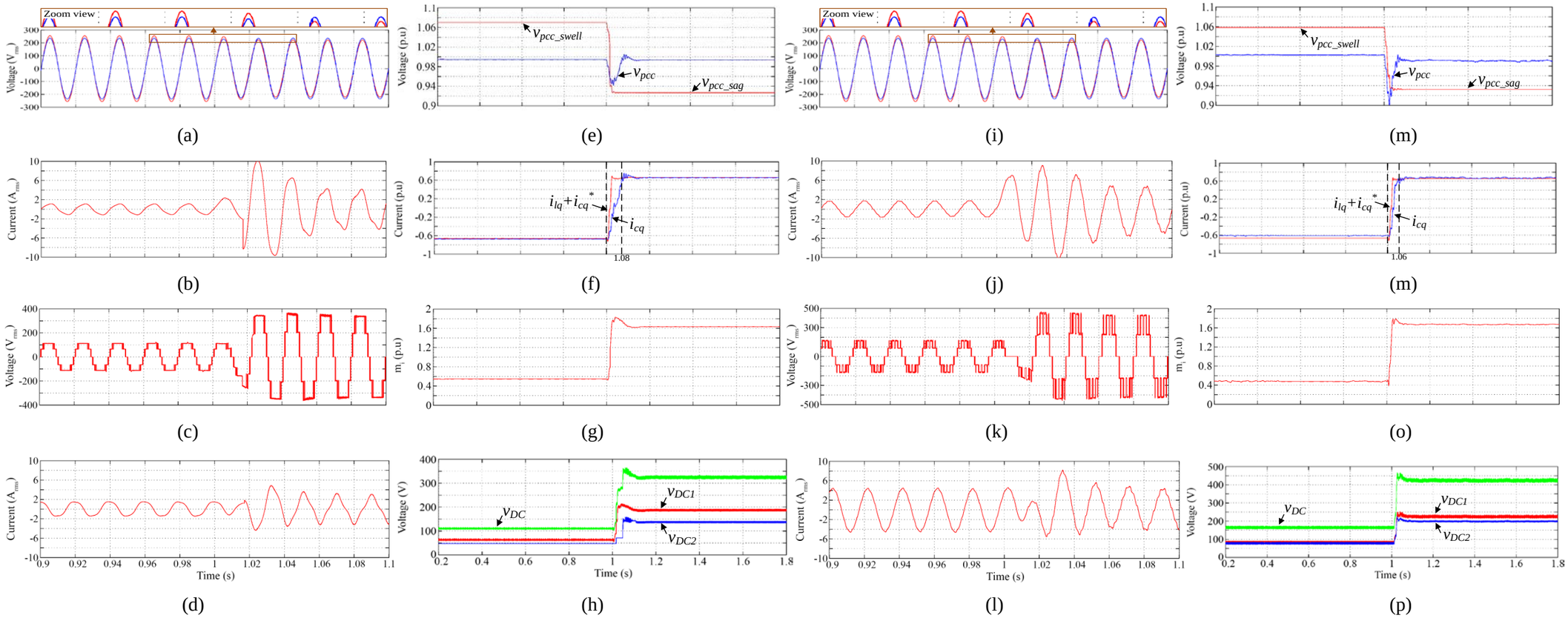

Figure 4-17. Case I (i.e., N_1/N_2 = 3/5): Simulation results of AC single-phase line-to-neutral

(a) grid voltage v_{pcc},

(b) grid current i_s,

(c) STATCOM voltage v_c,

(d) STATCOM current i_c,

and DC quantities of (e) grid voltage magnitude v_{pcc},

(f) ramp change of measured i_{cq} and reactive current references $i_{lq} + i_{cq}^*$,

(g) modulation indexes m_i, and

(h) boost converters output voltages v_{DC1} and v_{DC2} at different loading conditions.

Figure 4-18. Case II (i.e., N_1/N_2 = 3/8): Simulation results of AC single-phase line-to-neutral

(i) grid voltage v_{pcc},

(j) grid current i_s,

(k) STATCOM voltage v_c,

(l) STATCOM current i_c,

and DC quantities of (m) grid voltage magnitude v_{pcc},

(n) ramp change of measured i_{cq} and reactive current references $i_{lq} + i_{cq}^*$,

(o) modulation indexes m_i, and

(p) boost converters output voltages v_{DC1} and v_{DC2} at different loading conditions.

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Figure 4-17(f) shows the characteristic of the STATCOM reactive current i_{cq} which is consistently tracking the ramp-change of the load reactive current i_{lq}. Similar observation is also seen from Figure 4-17(h), where the dynamic and steady-state characteristics of each DC output voltage (i.e., v_{DC1} and v_{DC2}) in response to the resultant modulation index m_i (see Figure 4-17(g)) provided by the proposed control scheme is demonstrated.

The performance of the MSHE-PWM based STATCOM system under Case II is also investigated and as expected a better dynamic response is observed as shown in Figure 4-17. However, this is at the cost of higher switching frequency (i.e., 2.2 kHz compared to 1.6 kHz) which increases the switching losses. Nevertheless, this is still comparably less than the typical frequency of CB-PWM technique [9], [55], [154], [185].

4.4.2.2 Experiment Results

Similarly, the small scale low-voltage laboratory prototype based on single-phase five-level CHI based single-phase STATCOM with separated DC voltage sources (see Figure 4-19) is again analysed to validate the simulation and theoretical findings. The system parameters are tabulated in Table 4-5.

Table 4-5. System Parameters Used in the Experimental Work.

Single-phase power system parameters:
S_{base} = 90 VA, V_{base} = 60 V_{rms}, I_{base} = 1.5 A_{rms}, Z_{base} = 40 Ω
Fundamental frequency: f = 50 Hz Single phase power rating = 1 p.u. Single phase grid voltage: v_{pcc} = 1 p.u. Coupling resistor: R_f = 4 Ω = 0.1 p.u. Coupling inductor: L_f = 127 mH Coupling impedance: Z_f = 40 Ω = 1 p.u. Load A R_lC_l: S_{l_A} = 85 W = 0.94 p.u., P_{l_A} = 60 W = 0.67 p.u., Q_{l_A} = 60 VAR = 0.67 p.u. Load A current: i_{l_A} = 1.4 A_{rms} = 0.94 p.u. Load B R_lL_l: S_{l_B} = 85 W = 0.94 p.u., P_{l_B} = 60 W = 0.67 p.u., Q_{l_B} = 60 VAR = 0.67 p.u. Load B current: i_{l_B} = 1.4 A_{rms} = 0.94 p.u.

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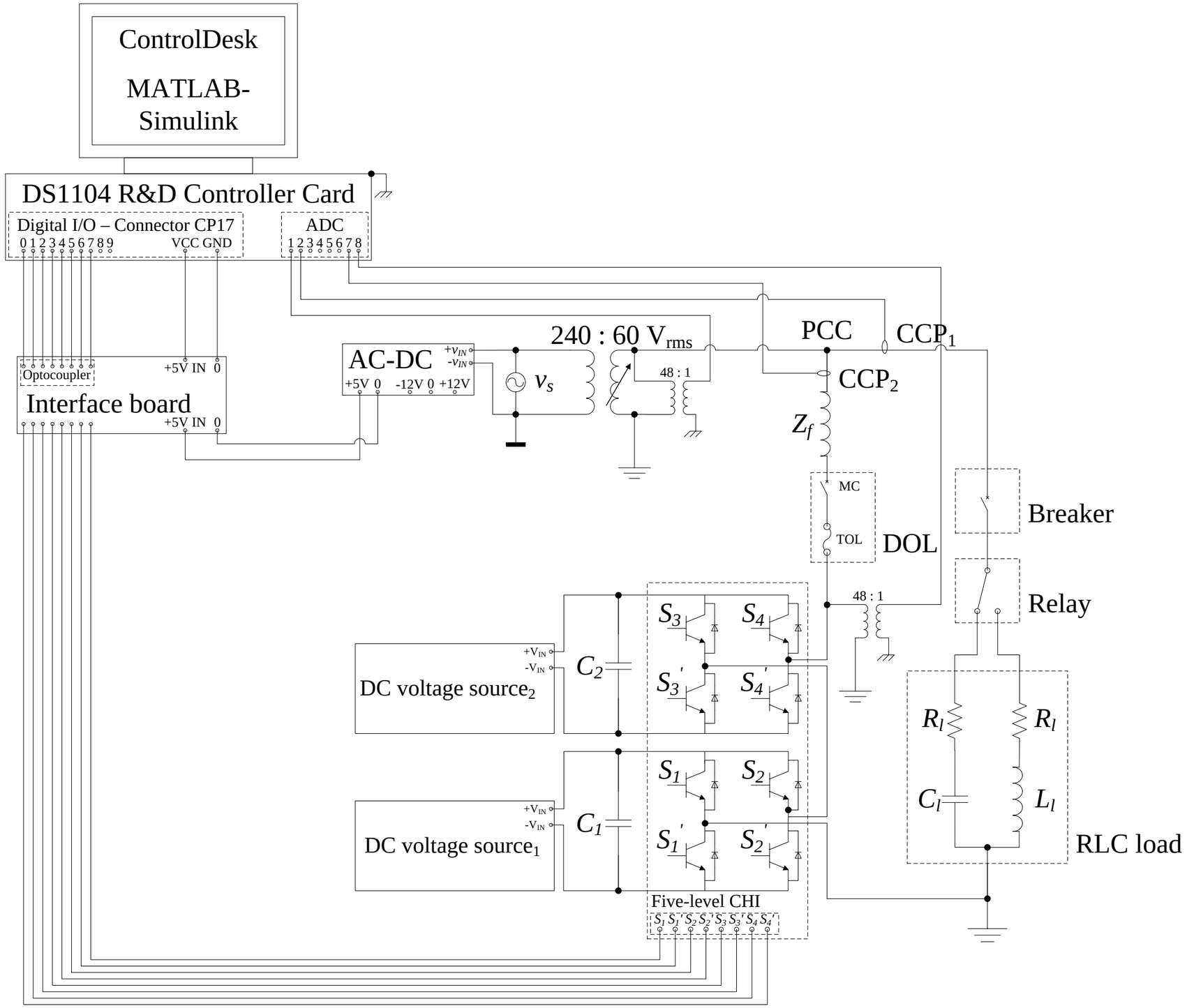

Figure 4-19: Circuit diagram of five-level SHE-PWM (i.e., Case II (i.e., N_1/N_2 = 3/8) H-bridge inverter based single-phase STATCOM with the separated DC voltage sources.

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Selected results are chosen to investigate the dynamic, transient, and harmonics performances of the proposed MSHE-PWM method. The results are discussed in the following subsections.

The real-time line-to-neutral five-level SHE-PWM output voltage waveform (i.e., for Case II) and the associated spectra are shown in Figure 4-20, which is in a good match with the simulation results presented in Figure 4-16. Once again, it is confirmed that the proposed MSHE-PWM method offers a tight control of the low-order non-triplen harmonics for the full range of the inverter operation.

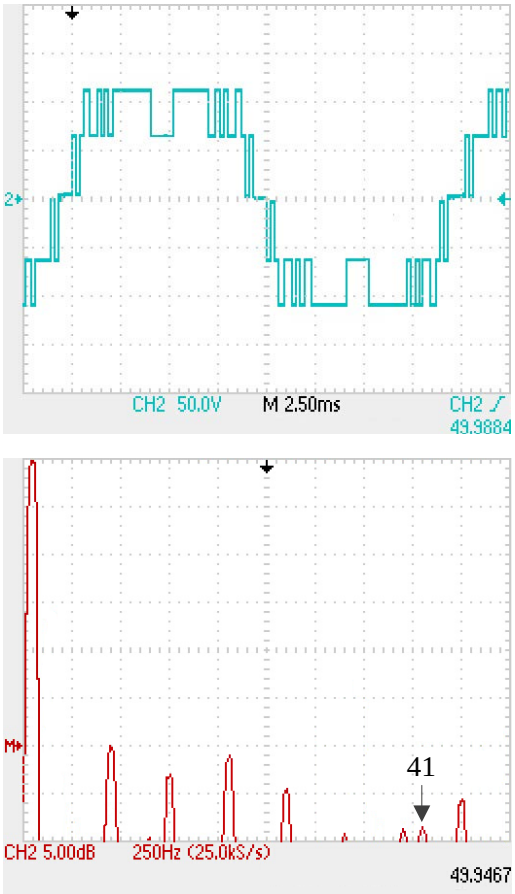
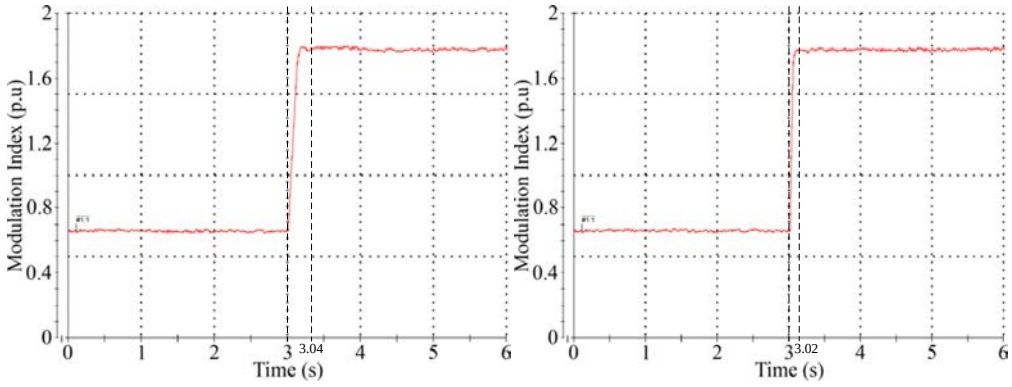


Figure 4-20. Experimental implementation of line-to-neutral five-level SHE-PWM (i.e., N_1/N_2 = 3/8) output voltage waveform and the associated spectrum.

Figure 4-21 illustrates the dynamic difference between both cases of the MSHE-PWM based STATCOM system at different loading conditions.



(a) (b)

Figure 4-21. Experimental results of modulation indexes m_i in p.u. value (a) Case I (i.e., N_1/N_2 = 3/5) and (b) Case II (i.e., N_1/N_2 = 3/8) at different loading conditions.

As expected, more switching instants exhibit a better dynamic response (i.e., for Case II as shown in Figure 4-21(b)) due to higher switching frequency and better inverter bandwidth; however, causing more switching losses when compared with Case I (see Figure 4-21(a)).

4.5 Summary

A novel transformer-less STATCOM controller based on a new version of MSHE-PWM control technique implementable with the CHI topology was investigated and proposed in this chapter. The proposed formulation of the MSHE-PWM method provides an output with a wider range of m_i by making the DC voltage-levels variant without affecting the number of harmonics being eliminated. It further provides constant switching angles and linear pattern of DC voltage-levels over the full range of the m_i which in turns eliminates the tedious steps of the off-line calculations of switching angles and eases the implementation of the MSHE-PWM for dynamic systems such as STATCOM. The effectiveness of the MSHE-PWM technique was first demonstrated by comparing it to the conventional IPD CB-PWM technique operated with the same switching frequency (i.e., 1.6 kHz) and applied to the same single-phase STATCOM system. Then, the performance of the proposed control scheme was investigated with different effective switching frequencies of the inverter (i.e., 1.6 kHz and 2.2 kHz)

achieved by different MSHE-PWM distribution ratios. Different loading conditions were considered in both simulation and experimental studies and it was found that the proposed MSHE-PWM technique outperforms the latter in many aspects such as output voltage harmonic profile (THD), response time, and steady-state performances. Furthermore, good responses were achieved by the proposed control scheme in both cases, where a high effective switching frequency reflects to better dynamic and transient responses but at the cost of increases the switching losses. Variable DC voltage-levels were obtained through a simple DC-DC converter, where the advancement and the rapid development in power semiconductors devices and advanced materials promised high efficiency DC-DC conversion systems.

The next chapter introduces the proposed three-phase STATCOM controller based on the new version of MSHE-PWM control technique to an unbalanced power system.

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Chapter 5 New Current Control Algorithm Incorporating Multilevel SHE-PWM Approach for STATCOM Operation under Unbalanced Condition

5.1 Introduction

This chapter extends the benefits of the new decoupling feed-forward current vector controllers (i.e., as proposed in Chapter 3) to three-phase STATCOM system that operates under unbalanced condition. The STATCOM is constructed using MCHI with separated DC-DC buck converters employing new MSHE-PWM technique (i.e., as reviewed in Chapter 4). Current vector controllers based on SRF are used to separately regulate the required positive- and negative-sequence variables to correct the PF and balance the three-phase grid currents at the PCC, respectively. The dynamic and the transient performances of the proposed approach are verified through various simulation studies.

The rest of this chapter is organized as follows: Section 5.2 presents the analysis and the formulation of the proposed STATCOM system along with its control. Simulation validated results are reported in Section 5.3. Finally, conclusions are summarized in Section 5.4.

5.2 The Proposed Three-Phase STATCOM: Key Operation

The circuit structure of three-phase five-level CHI is shown in Figure 5-1, while the typical quarter-cycle MSHE-PWM equations with a distribution ratio of N_1/N_2 = 3/5 have been presented in Chapter 4 under Section 4.2. Figure 5-2 shows the single-line block diagram of the three-phase STATCOM system based on the proposed five-level SHE-PWM inverter along with the associated proposed control scheme. The state-space averaging model of the DC-DC buck converter proposed in Chapter 4 under Section 4.3.1 is employed in this work to control the DC-link voltage-levels based on the corresponding m_i.

From Figure 5-2, the STATCOM main system incorporated with the new decoupling feed-forward current control algorithm (i.e., as proposed in Chapter 3) is employed to correct the low grid PF and compensate the unbalanced conditions at the grid side. Specifically, the decoupling feed-

forward current vector controller based positive SRF rotating at synchronous speed (i.e., $+\omega = 2\pi f$) are developed to control the positive-sequence components for providing PF correction at the PCC, whereas another decoupling feed-forward current vector controller based negative SRF (i.e., $-\omega$) is established to attain balanced grid currents i_s, hence balanced grid voltages v_{pcc}.

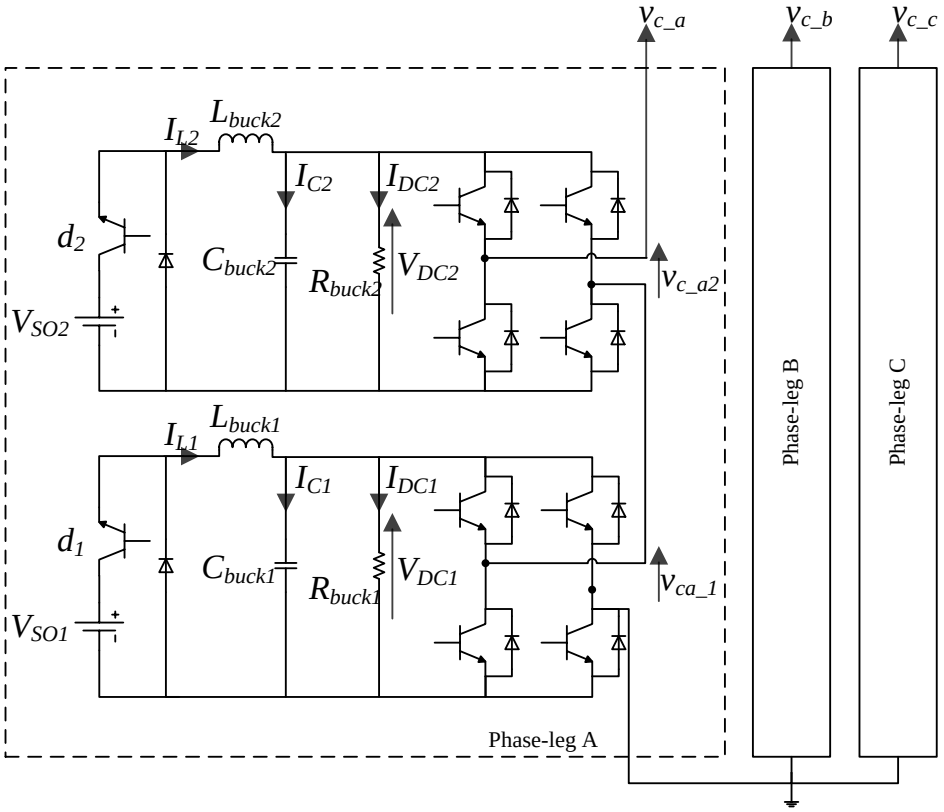

Figure 5-1. Three-phase five-level inverter with the associated DC-DC buck converters.

In general, three-phase voltages and currents at balanced condition can be represented as in (5-1) below:

$$\begin{bmatrix} v_{pcc\alpha} \\ v_{pccb} \\ v_{pccc} \end{bmatrix} = \begin{bmatrix} \sqrt{2}v_{pcc\alpha}\cos(\omega t) \\ \sqrt{2}v_{pccb}\cos\left(\omega t - \frac{2\pi}{3}\right) \\ \sqrt{2}v_{pccc}\cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} = \begin{bmatrix} v_{pcc\alpha} \\ \alpha \times v_{pccb} \\ \alpha^2 \times v_{pccc} \end{bmatrix} \quad (5\text{-}1)$$

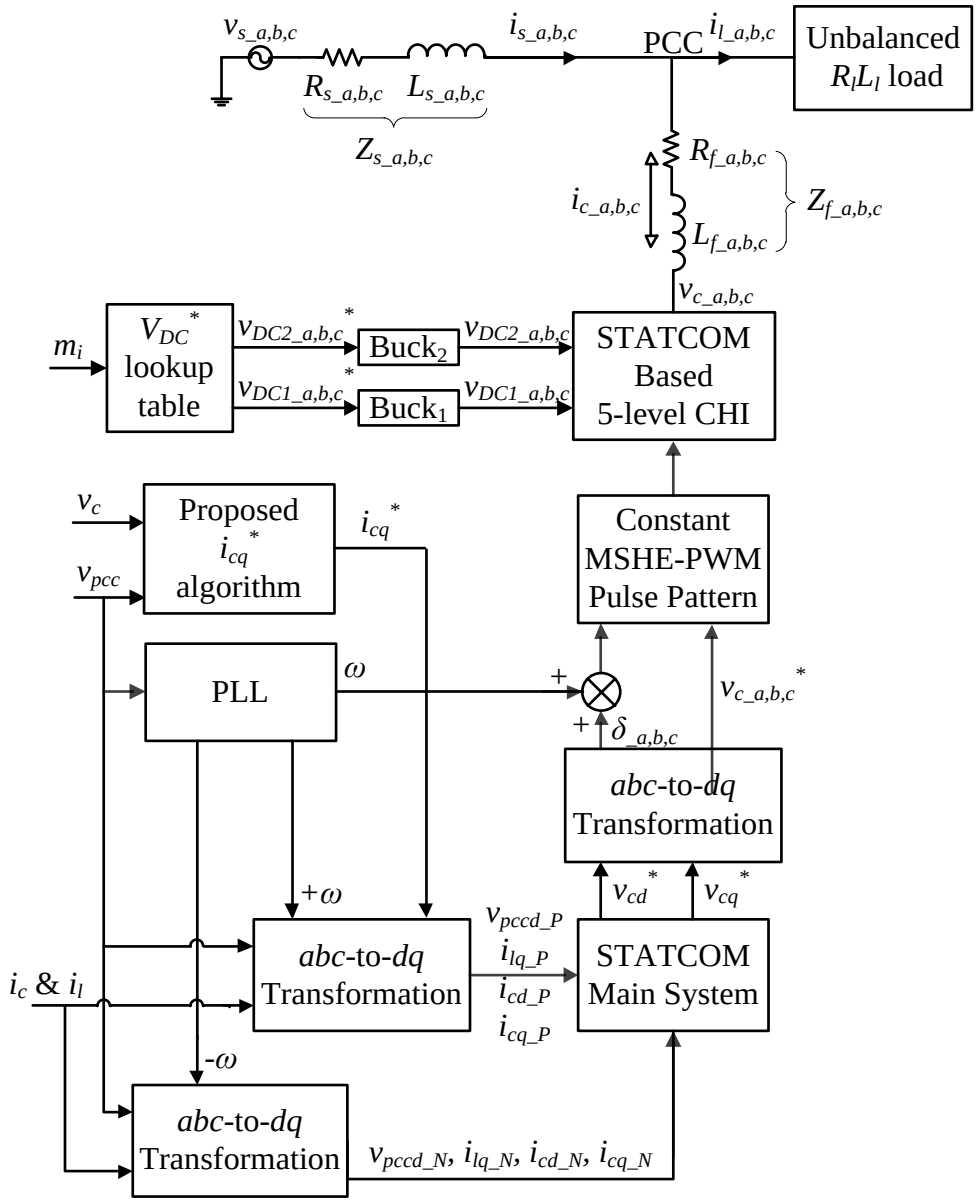

Figure 5-2. Block diagram of the three-phase STATCOM system with the associated proposed control scheme.

The positive- and negative-sequence components of (5-1) can be obtained by decomposing it via the Park's Transformation (see *abc*-to-*dq* transformation shown in Appendix B) with positive- (i.e., $+\omega$) and negative- (i.e., $-\omega$) SRF, respectively, as defined in (5-2) and (5-3) below.

$$\begin{bmatrix} v_{pc\alpha\_P} \\ v_{pccb\_P} \\ v_{pccc\_P} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix}\begin{bmatrix} v_{pc\alpha} \\ v_{pccb} \\ v_{pccc} \end{bmatrix} \tag{5-2}$$

$$\begin{bmatrix} v_{pcc\alpha\_N} \\ v_{pccb\_N} \\ v_{pccc\_N} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \alpha^2 & \alpha \\ \alpha & 1 & \alpha^2 \\ \alpha^2 & \alpha & 1 \end{bmatrix}\begin{bmatrix} v_{pcc\alpha} \\ v_{pccb} \\ v_{pccc} \end{bmatrix} \tag{5-3}$$

where $\alpha = 1\angle 120^\circ = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ and $\alpha^2 = 1\angle -120^\circ = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$.

The STATCOM system's transfer function in *dq*-coordinates is defined as follows:

$$\begin{bmatrix} v_{cd\_P/N} \\ v_{cq\_P/N} \end{bmatrix} = \begin{bmatrix} v_{pccd\_P/N} \\ v_{pccq\_P/N} \end{bmatrix} - R_f \begin{bmatrix} i_{cd\_P/N} \\ i_{cq\_P/N} \end{bmatrix} - L_f \frac{d}{dt}\begin{bmatrix} i_{cd\_P/N} \\ i_{cq\_P/N} \end{bmatrix} + \omega L_f \begin{bmatrix} i_{cq\_P/N} \\ -i_{cd\_P/N} \end{bmatrix} \tag{5-4}$$

By integrating (5-4) between the current sample (*k*) and (*k*+1) and then dividing it by the operating rates (i.e., T_{id} and T_{iq} for *d*- and *q*-axis current vector controller, respectively), the average magnitude of *dq*-voltage vectors from the sample period (*k*) to (*k*+1) are then derived as follows:

$$\begin{aligned} v_{cd\_P/N}(k,k+1) = {} & v_{pccd\_P/N}(k,k+1) + \omega L_f i_{cq\_P/N}(k,k+1) - R_f i_{cd\_P/N}(k,k+1) \\ & - \frac{L_f}{T_{id}}\left[i_{cd\_P/N}(k+1) - i_{cd\_P/N}(k) \right] \end{aligned} \tag{5-5}$$

$$\begin{aligned} v_{cq\_P/N}(k,k+1) = {} & v_{pccq\_P/N}(k,k+1) - \omega L_f i_{cd\_P/N}(k,k+1) - R_f i_{cq\_P/N}(k,k+1) \\ & - \frac{L_f}{T_{iq}}\left[i_{cq\_P/N}(k+1) - i_{cq\_P/N}(k) \right] \end{aligned} \tag{5-6}$$

Since fast and optimal current controller response is always of prime importance in STATCOM applications, therefore the STATCOM output currents at the next sample (i.e., $i_{cd}(k+1)$ and $i_{cq}(k+1)$) are set to track the current references at the current sample (i.e., $i_{cd}^*(k)$ and $i_{lq}(k)$) as follows:

$$i_{cd\_P/N}(k+1) = i_{cd\_P/N}^*(k) = 0 \tag{5-7}$$

$$i_{cq\_P/N}(k+1) = i_{lq\_P/N}(k) + i_{cq}^* \tag{5-8}$$

From (5-7), the active current reference $i_{cd\_P/N}^{*}(k)$ values for both the positive- and negative- sequence controllers are neglected because the DC-link voltage of each H-bridge inverter is provided by the DC/DC buck converter. In order to make the variation of (5-7) and (5-8) occur linearly between the two samples (k) and (k+1) during one sampling period (i.e. k to k+1),

$$i_{cd\_P/N}(k,k+1)=\frac{1}{2}i_{cd\_P/N}(k)+\frac{1}{2}i_{cd\_P/N}{}^{*}(k)=\frac{1}{2}i_{cd\_P/N}(k) \tag{5-9}$$

$$i_{cq\_P/N}(k,k+1)=\frac{1}{2}i_{cq\_P/N}(k)+\frac{1}{2}\left(i_{lq\_P/N}(k)+i_{cq}{}^{*}\right) \tag{5-10}$$

The grid voltage v_{pcc} and the STATCOM output voltage v_c are assumed to be constant and equal to its voltage reference within one sampling period (i.e., k to k+1) as follows:

$$v_{pccd\_P/N}(k,k+1)=v_{pccd\_P/N}(k) \tag{5-11}$$

$$v_{pccq\_P/N}(k,k+1)=v_{pccq\_P/N}(k) \tag{5-12}$$

$$v_{cd\_P/N}(k,k+1)=v_{cd\_P/N}{}^{*}(k) \tag{5-13}$$

$$v_{cq\_P/N}(k,k+1)=v_{cq\_P/N}{}^{*}(k) \tag{5-14}$$

By substituting (5-7)-(5-14) into (5-5) and (5-6), the resultant dq positive- and negative-sequence voltage reference values are obtained as follows:

$$\begin{aligned}v_{cd\_P/N}{}^{*}(k)=v_{pccd\_P/N}(k)-R_f i_{cd\_P/N}(k)-K_{p\_id}\left[-i_{cd\_P/N}(k)\right]\\+\frac{\omega L_f}{2}\left[i_{cq\_P/N}(k)+\left(i_{lq\_P/N}(k)+i_{cq}{}^{*}\right)\right]\end{aligned} \tag{5-15}$$

$$\begin{aligned}v_{cq\_P/N}{}^{*}(k)=v_{pccq\_P/N}(k)-R_f i_{cq\_P/N}(k)-\frac{\omega L_f}{2}\left[i_{cd\_P/N}(k)\right]\\-K_{p\_iq}\left[\left(i_{lq\_P/N}(k)+i_{cq}{}^{*}\right)-i_{cq\_P/N}(k)\right]\end{aligned} \tag{5-16}$$

where the proportional gain $K_{p\_i(d,q)}$ of the P-controller is given by:

$$K_{p\_i(d,q)} = \frac{L_f}{T_{i(d,q)}} + \frac{R_f}{2} \tag{5-17}$$

Hence, the desired STATCOM output voltage magnitude v_c^* and its phase angle δ with respect to v_{pcc} is given as follows:

$$v_c^* = \sqrt{(v_{cd\_P}^* - v_{cd\_N}^*)^2 + (v_{cq\_P}^* - v_{cq\_N}^*)^2} = \sqrt{(v_{cd}^*)^2 + (v_{cq}^*)^2} = m_i \tag{5-18}$$

$$\delta = tan^{-1}\left(\frac{v_{cq}^*}{v_{cd}^*}\right) \tag{5-19}$$

5.3 Results and Discussion

The proposed three-phase STATCOM system (see model in Appendix M) under unbalanced condition is investigated using Matlab/Simulink software package for the system parameters tabulated in Table 5-1. The unbalanced condition is created by three unevenly distributed single-phase R_lL_l loads over the phases. The real-time implementation of the buck converter and its associated voltage loop feedback control are shown in Appendix F and Appendix G, respectively.

Figure 5-3 presents the dynamic and transient responses of the three-phase STATCOM system in response to the unbalanced load condition. From Figure 5-3, between 0.3 to 0.5 seconds, only the decoupling feed-forward current vector controller based positive SRF is applied to control the positive-sequence variables in order to correct the grid PF. From 0.51 onwards, the compensation of negative-sequence variables is then added with the former controller to balance the three-phase grid currents as shown in Figure 5-3(a). Figure 5-3(d) and Figure 5-3(e) illustrate that both the positive- and negative-sequence components of the STATCOM reactive current i_{cq} are consistently tracking the load reactive current i_{lq} reference value. Figure 5-3(f) and Figure 5-3(g) demonstrate the dynamic performance of the proposed MSHE-PWM based STATCOM system, which took approximately 4 cycles to rebalance the grid currents and reaching steady-state (i.e., similar performance as shown in Figure 4-13(a)).

Table 5-1. System Parameters Used in the Simulation Study.

Buck converter steady-state parameters:
DC voltage source: V_{so} = 240 V Switching frequency: f_{sw_buck} = 2 kHz Filter inductor: L_{buck} = 500 µH Filter capacitor: C_{buck} = 250 µF Filter resistor: R_{buck} = 1 Ω Crossover frequency: ω_{cross_buck} = 5657 rad/s Gain of error amplifier A = 36.66 Zero-frequency: ω_{z_buck} = 752.24 rad/s Pole-frequency: ω_{p_buck} = 742539.51 rad/s
Single-phase power system parameters:
S_{base} = 1.44 kVA, V_{base} = 240 V_{rms}, I_{base} = 6 A_{rms}, Z_{base}= 40 Ω Fundamental frequency: f = 50 Hz Single phase power rating = 1 p.u. Single phase grid voltage: v_{pcc} = 1 p.u. Grid resistor: R_s = 0.4 Ω = 0.01 p.u. Grid inductor: L_s = 12.7 mH Grid impedance: Z_s = 4 Ω = 0.1 p.u. Coupling resistor: R_f = 4 Ω = 0.1 p.u. Coupling inductor: L_f = 127 mH Coupling impedance: Z_f = 40 Ω = 1 p.u. Phase A R_lL_l load: R_{l_a} = 60 Ω = 1.5 p.u. L_{l_a} = 0.1 H = 0.0025 p.u. Phase A load current: i_{l_a} = 3.6 A_{rms} = 0.6 p.u. Phase B R_lL_l load: R_{l_b} = 60 Ω = 1.5 p.u. L_{l_b} = 0.2 H = 0.005 p.u. Phase B load current: i_{l_b} = 2.8 A_{rms} = 0.46 p.u. Phase C R_lL_l load: R_{l_c} = 60 Ω = 1.5 p.u. L_{l_c} = 0.3 H = 0.0075 p.u. Phase C load current: i_{l_c} = 2.2 A_{rms} = 0.36 p.u. d-axis Proportional gain: K_{p_id} = 0.21 q-axis Proportional gain: K_{p_iq} = 1.63 d-axis operating rate: T_{id} = 0.02 q-axis operating rate: T_{iq} = 0.002 d-axis operating rate: T_{vd} = 0.02

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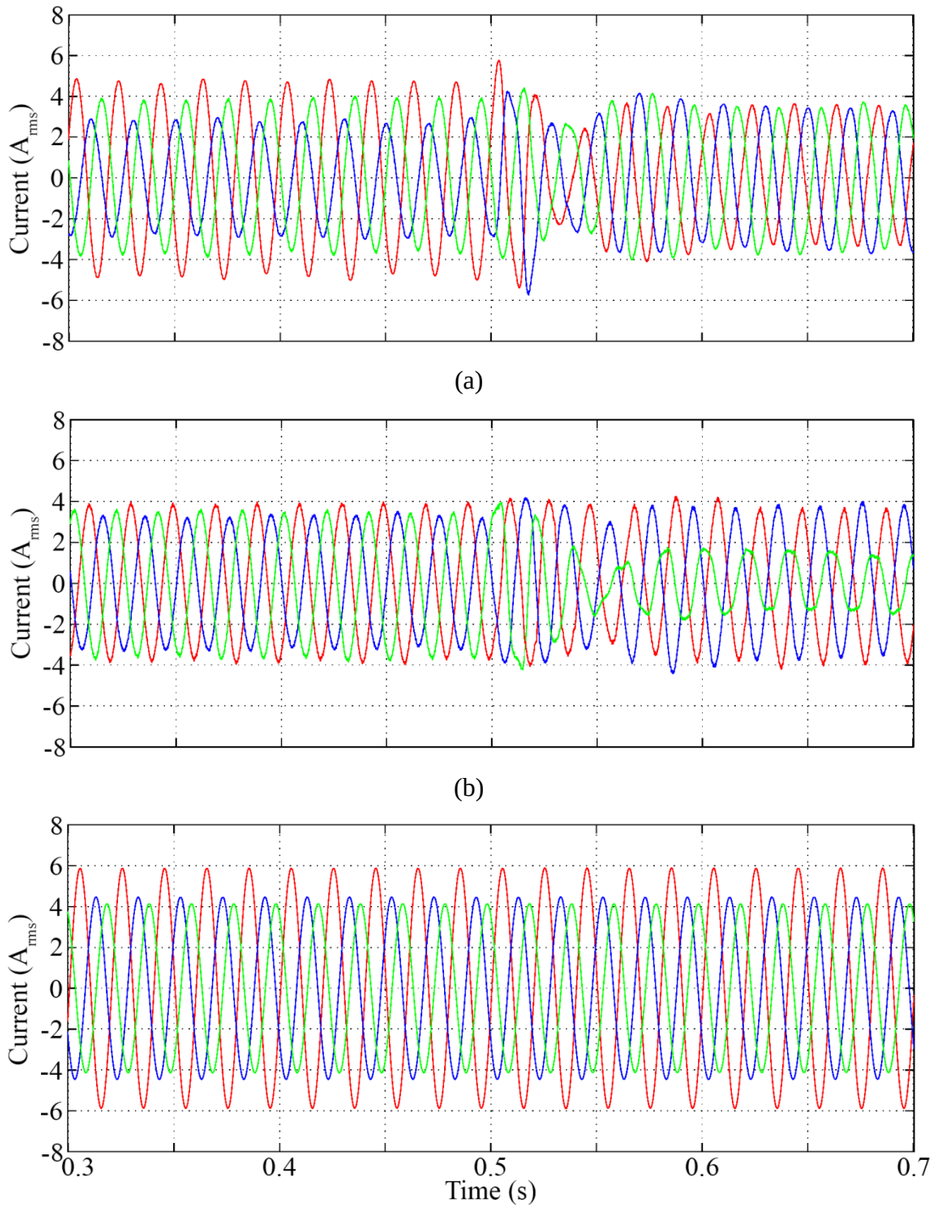

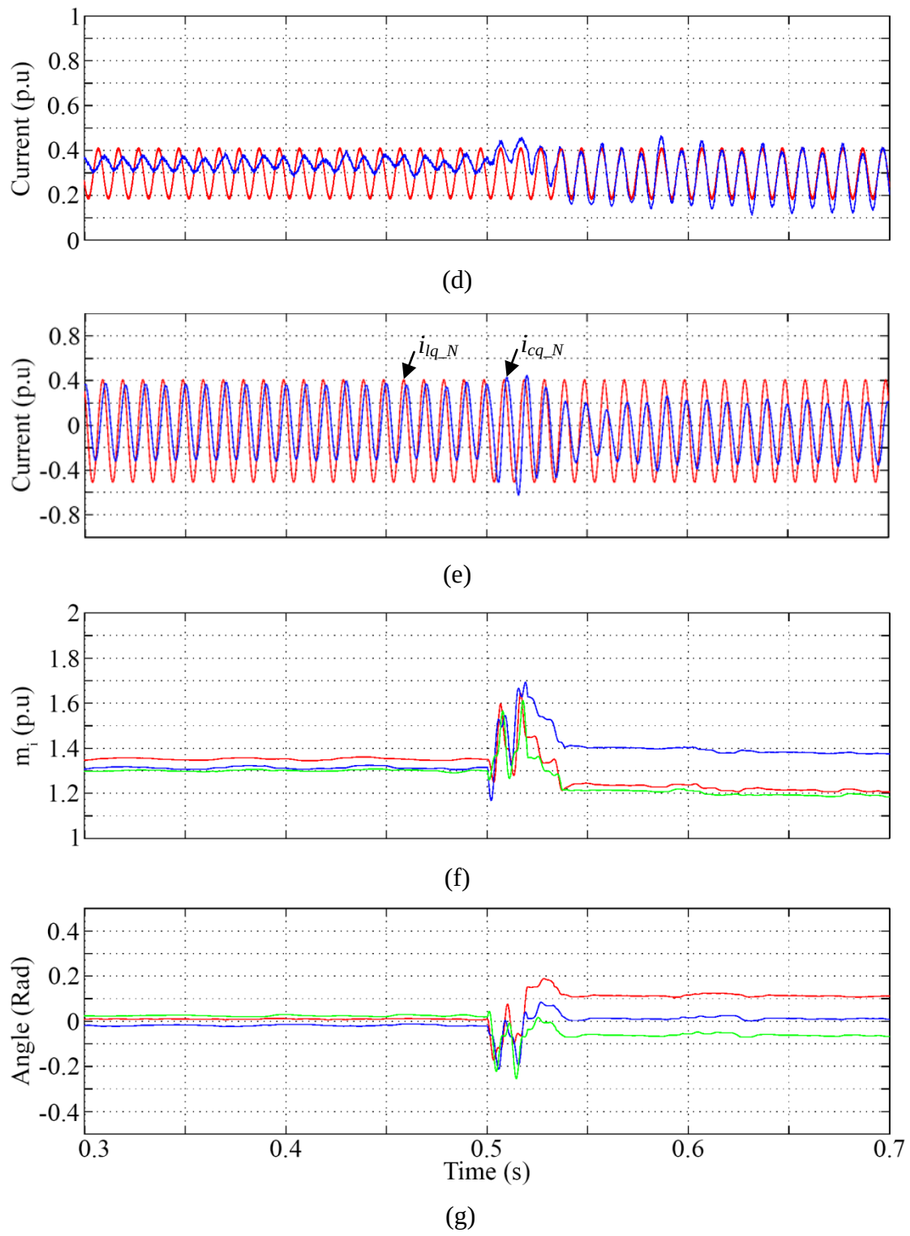

Figure 5-3. Simulation results of STATCOM operating under unbalanced load condition (a) grid current i_s, (b) STATCOM output current i_c, (c) load current i_l, (d) positive-sequence components of STATCOM output reactive current i_{cq_P} and load reactive current i_{lq_P}, (e) negative-sequence components of STATCOM output reactive current i_{cq_N} and load reactive current i_{lq_N}, (f) resultant modulation indexes m_i, and (g) resultant phase angle δ.

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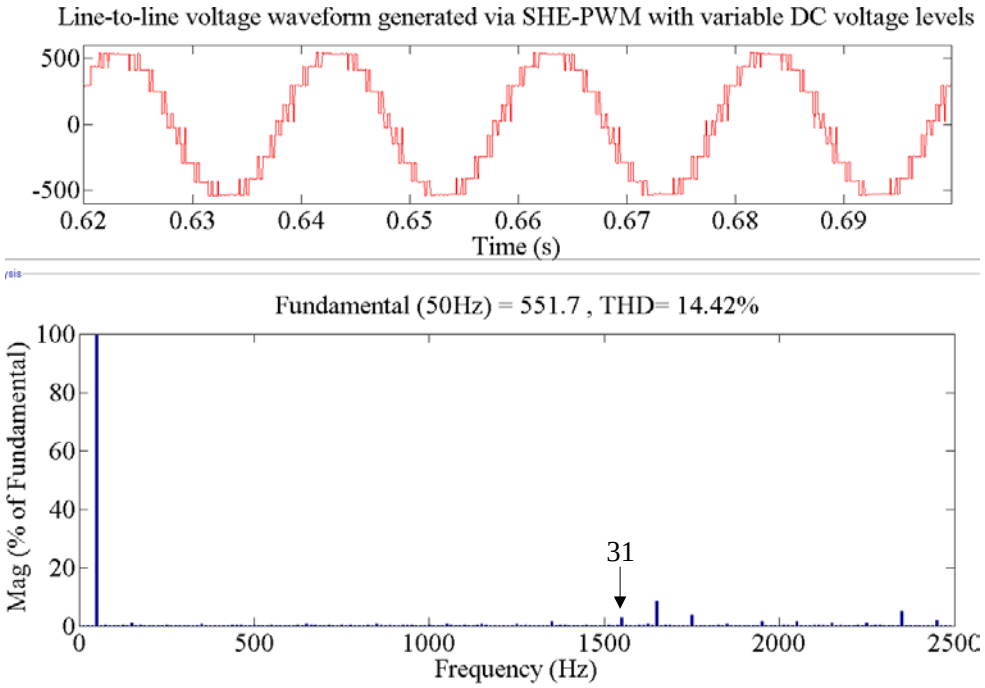
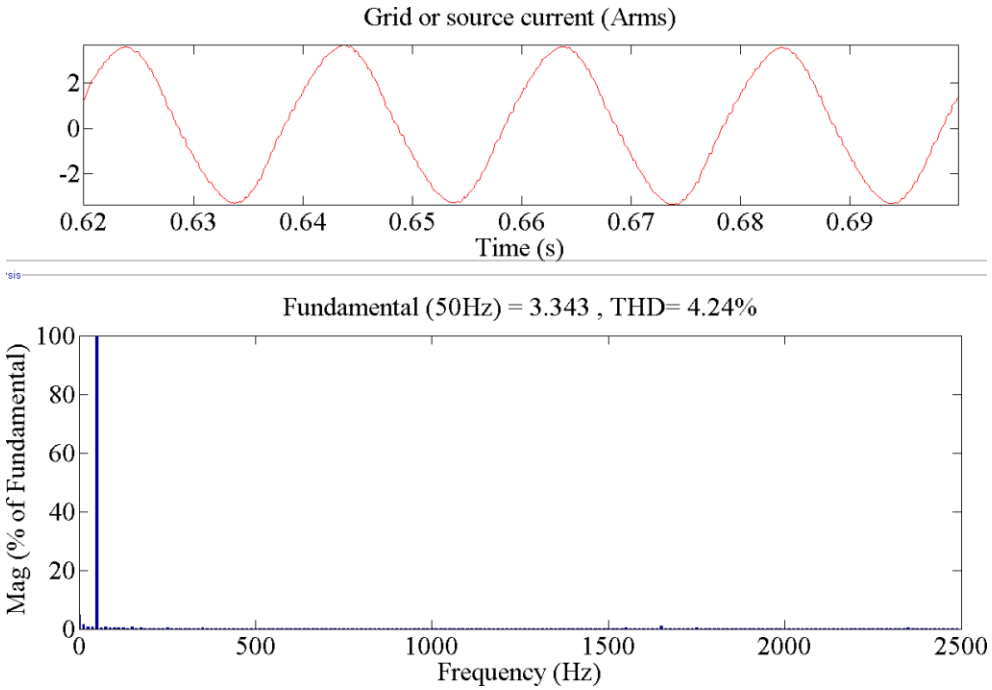
The implementation of the line-to-line STATCOM output voltage v_c and grid current i_s waveforms are illustrated in Figure 5-4(a) and Figure 5-4(b), respectively, along with its associated spectra.



(a)



(b)

Figure 5-4. Simulation results of line-to-line (i.e., Phase A to Phase B) (a) MSHE-PWM output voltage v_c waveform and its spectrum and (b) grid current i_s waveform and its spectrum.

Recalling from Figure 4-7 that the proposed line-to-neutral five-level SHE-PWM voltage waveform eliminates nine low-order non-triplen harmonics and the next harmonic appears in the spectrum is the 31st. This is reflected on the line-to-line STATCOM output voltage v_c and grid current i_s as shown in Figure 5-4(a) and Figure 5-4(b), respectively. Furthermore, triplen harmonics (i.e. 3rd, 9th, 15th, 21st, 27th, 33rd and etc.) are absent in three-phase system as shown in Figure 5-4(a) when compared it with Figure 4-7.

5.4 Summary

This chapter has investigated the performance of the proposed STATCOM system under three-phase unbalanced load. The use of DC-DC buck converters as voltage source for the five-level CHI increases the compensation degree of the unbalance due to the capability to supply active current to the PCC. To enable a simpler control design, both the positive- and negative-sequence components of these variables (i.e., grid voltage v_{pcc}, load current i_l, and STATCOM output current i_c) were extracted and then separately regulated by the proposed decoupling feed-forward current vector controllers to achieve fast and stable operating performance. Besides that, the proposed formulation of the MSHE-PWM method provides an improved output voltage quality with a wider range of m_i by making the DC voltage-levels variant without affecting the number of harmonics being eliminated. Selected simulation results were presented to demonstrate the effectiveness of the proposed approaches.

Chapter 6 Conclusions and Recommendations for Future Works

6.1 Conclusions

Voltage Source Inverters (VSIs) are the key technology behind advanced power electronics applications associated with modern power systems devices such as STATCOM and other FACTS controller. Various VSI topologies are presented in this dissertation and the multilevel inverters have gained wide interest and attention in recent years in high-voltage high-power applications due to their inherent advantages [25]-[28]. The dissertation investigated different multilevel circuit topologies, documenting their features, advantages, and disadvantages. MCHI was found an attractive topology for high-voltage high-power applications including STATCOM system due to their modularization, extensibility, and control simplicity. Nevertheless, there have been many challenges associated with MCHI aiming to achieve a high bandwidth current control with a low switching frequency and minimum output harmonics being able to effectively track the demand signal.

This dissertation also presented the most commonly applied modulation techniques and control schemes to MCHI based STATCOM application. The advantages and disadvantages of these methods were also discussed and their implementation was briefly reviewed. Particularly, the feed-forward/feedback control scheme based on *dq*-method (i.e., as reviewed in under Section 2.2.2.4) offers adequate dynamic and tolerable transient characteristic in response to a step change of the loading conditions. However, the controller's gain parameters were not specifically defined [31]-[33] and moreover, details on the modulation technique as well as the employment of both the sampling and switching frequencies are not thoroughly discussed [42], [45], [46]. On the other hand, the PI-controllers have been considered as the simplest way to perform control actions in the feedback loops. However, several works have revealed that the PI-controllers could not provide precise tracking of the command values [9] due to the variations of parameters and operating points [40], [45] that leads to poor transient response and instability of the STATCOM system [48]. Moreover, methods to remedy the issues involve high-switching frequency (i.e., 5 kHz [154], 10 kHz [9] and [185]) to

attain the desired current loop bandwidth as well as complicated rules and factors to relate the input variables to the output model properties [45]-[46].

The MSHE-PWM technique (i.e., as presented in Chapter 2 under Section 2.2.2.3) offers significant advantages compared with the conventional CB-PWM technique. These include acceptable performance with low-switching frequency ratio to fundamental frequency ratio, tight control over output waveform harmonics, and the ability to leave triplen harmonics uncontrolled to take advantage of circuit topology in three-phase system. For these reasons, MSHE-PWM technique remains the hot topic for high-voltage high-power VSIs, where the constant switching transitions/angles being able to increase the inverter bandwidth and reduce or eliminate maximum number of harmonics with relatively low switching frequency. This dissertation extended the features and benefits of the new MSHE-PWM technique proposed by Dahidah et al. [98] to the STATCOM system controlled by the proposed control scheme. It is worth noting that the new MSHE-PWM technique considers variable DC voltage-levels enabling more harmonics to be eliminated (i.e., (N+M)-1) compared to N-1) for the conventional MSHE-PWM technique with constant DC voltage-levels, where N is the total switching angles per quarter cycle and M is the total number of H-bridge inverters per phase-leg.

This dissertation proposed a decoupling feed-forward current vector controller based on the *dq*-method to provide VAR compensation and PF correction under different loading conditions. To exhibit a rapid correction response, P-controllers were employed to achieve both fast and robust control of the reactive current. On the other hand, a new reactive current reference i_{cq}^{*} algorithm given by (3-34) was also proposed to provide an opposite signal to the decoupling feed-forward current controller in response to the variation of the STACOM reactive current i_{cq} during the steady-state condition. This in turns improves steady-state performance of the STATCOM system without using any integral functions or filters in the feedback control loop.

The proposed control scheme (i.e., decoupling feed-forward current vector controller incorporating a new reactive current reference i_{cq}^{*} algorithm) is applied to both the CB-PWM (see Chapter 3) and MSHE-PWM (see Chapter 4) techniques to control the MCHI based STATCOM with equal and

variant DC voltage-levels, respectively. Specifically, Chapter 3 demonstrated the capability of the proposed control scheme that enhanced the transient response and the steady-state error of the STATCOM reactive current i_{cq} for the given reactive loading conditions (see Figure 3-7 and Figure 3-13) while retaining good dynamic performance with low-switching frequency (i.e., 1.6 kHz).

Chapter 4 illustrated the effectiveness the new MSHE-PWM technique against the conventional IPD CB-PWM technique (i.e., employed in Chapter 3) operated with the same switching frequency (i.e., 1.6 kHz) and applied to the same STATCOM system. The new MSHE-PWM method provides constant switching angles and linear pattern of DC voltage-levels over the m_i range, easing the implementation of the MSHE-PWM for dynamic systems. Furthermore, it was also found that the proposed MSHE-PWM technique outperforms the CB-PWM in many aspects such as tight control of low-order harmonics (see Figure 4-7, Figure 4-9, and Figure 4-14) as well as better dynamic and steady-state response time (i.e., 50% improvement) as shown in Figure 4-10 and Figure 4-13. Chapter 4 has further investigated the performance of MSHE-PWM based STATCOM system with different effective switching frequencies of the inverter (i.e., Case I: 1.6 kHz and Case II: 2.2 kHz). It was found that a high effective switching frequency offers to better dynamic and transient responses (i.e., 5 cycles improvement as shown in Figure 4-17 and Figure 4-17) but at the cost of increasing switching losses. Nevertheless, when compared to the CB-PWM based STATCOM with a typical switching frequency ranges between 5 kHz [154] and 10 kHz [185], the proposed MSHE-PWM method offers less losses and less cooling and low power dissipation requirement, which could considerably reduce the volume and weight of the overall system and hence, increase its reliability and performance.

The effectiveness of both the proposed control scheme and the MSHE-PWM technique was verified again in Chapter 5 under three-phase unbalanced condition. The unbalanced condition was created by three unevenly distributed single-phase R_lL_l loads over the phases. The decoupling feed-forward current vector controllers based SRF (i.e., $+\omega$ and $-\omega$) were employed to separately regulate the required positive- and negative-sequence variables for correcting

the grid PF (see Figure 5-3(d)) and balancing the three-phase grid currents (see Figure 5-3(a)) at the PCC, respectively. Recalling that a DC-DC converter is used to feed the variable DC voltage-levels for each H-bridge cell according to the m_i, hence no DC voltage loop feedback control is required to regulate the DC-link voltages. The dynamic performance of the proposed control scheme was illustrated in Figure 5-3(f) and Figure 5-3(g), where it took approximately 4 cycles to rebalance the grid currents and reach steady-state (i.e., similar performance as shown in Figure 4-13(b)). Nevertheless, it is worth noting that the proposed control scheme with DC voltage loop feedback offers almost instantaneous dynamic response as shown in Figure 3-7 and Figure 3-13 in Chapter 3.

These simulation studies is carried out using Matlab/Simulink 2009b software package and the results were experimentally validated and verified using a single-phase laboratory prototype (i.e., rated at around 1.44 kW) controlled by dSPACE DS1104 processor board (see Chapter 3 under Section 3.4.2). Loading condition was altered using a switchable *RLC* load bank connected at the PCC. A good match between experimental and simulation results were achieved.

6.2 Suggestions for Future Works

This work aimed to proposed an effective control solution which can improve the existing ones (i.e., [9], [31]-[59]); thus, the experimental work was conducted using the existing single-phase five-level CHI rig and the processor board only. As a result, only the line-to-neutral waveforms (i.e., one-leg of the three-phase) were shown. However, implementing a three-phase power rig is recommended in future work for balanced, unbalanced, and fault conditions.

This dissertation has also reported that the MSHE-PWM technique could eliminate more number of harmonics if the DC voltage-levels are made variable. However, setting up variable voltage converters is out of the scope of this dissertation. Nevertheless, efforts have been made to design the voltage closed loop controllers of both the DC-DC buck- and boost-type converter, which employed in conjunction with MCHI topology for providing reactive

current compensation. Future work can be carried out to implement DC-DC converters or alike in practical by taking into system efficiency, characteristic performance, and size of passive components into consideration.

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Appendix A Examples of STATCOM installations worldwide

Year	Location	Country	Ratings (MVAR)	Remarks
1987	Ichikawa Works	Japan	±5	GTO
1988	Yokohama	Japan	±5	GTO
1990	Kochi	Japan	+0.4	IGBT
	Ohmiya	Japan	+0.75	IGBT
	Shinnannyou Works	Japan	±20	GTO
1991	Inumaya	Japan	±80	48-pulse VSI
	Okayana Works	Japan	±49.5	GTO
	Tokyo Works	Japan	±15	GTO
1992	Shin Shinano	Japan	±50	GTO, 2-level VSI
	Teine	Japan	±20	GTO
1993	Mitomi	Japan	+0.5	IGBT
	Shintakatsuka	Japan	±48	GTO
1994	Mukoyama Works	Japan	±22	GTO
	Shibukawa Works	Japan	±16.5	GTO
1995	Chita Works	Japan	±27	GTO
	Kinuura Works	Japan	±18	GTO
	Sullivan Substation	USA	±100	GTO, 48-pulse VSI, [13], [14]
1996	Karisaka	Japan	+1.5	IGBT
	Tobishima	Japan	+0.32	IGBT
1997	Rejsby Hede	Denmark	+16	IGBT, 12-pulse inverter
	Seguin, Texas Plant	USA	±80	GTO, 48-pulse inverter
	Inez Station, Kentucky	USA	±160	GTO, 48-pulse inverter, [15], [16]
	Ube	Japan	±18	GTO
	Uddeholm Tooling	Sweden	+44	VSI
1998	Hachinohe	Japan	±18	GTO
	Misato	Japan	±1.6	IGBT
	Oyama	Japan	±18	GTO
	Oyama	Japan	±27	GTO
	Paul Sweet Substation	USA	+60/-20	GTO, 24-pulse inverter

1999	Central and South West Corp	USA	±72	Three-level VSI
1999	Henan	China	+20	GTO, 24-pulse inverter, [17]
2000	Seattle Iron & Metals Corp.	USA	±2	IGBT, [13]
	Outokumpu	Finland	+164	VSI
	Saiko Lake	Japan	±1	IGBT
2001	East Claydon	United Kingdom	+225	GTO, [21]
	Kishiwada	Japan	±21	IEGT
	Mutu	Japan	+5/-3	IGBT
	Pohang	Korea	+30/-10	IEGT
	Société Nationale des Chemins de fer Français	France	±16	VSI
	VELCO Essex	USA	+133/-41	GCT, [19]
2002	Esashi	Japan	±0.5	IGBT
	Ichikawa	Japan	±21	IEGT
	Nagoya	Japan	±1.5	IGBT
	Shimokita	Japan	+11/-6	IGBT
	Shunan	Japan	±21	IEGT
	San Diego Gas & Electric	USA	±100	GCT, 3-level inverter, [22]
2003	Fujinomiya	Japan	±1	IGBT
	Kihoku	Japan	+2/-1	IGBT
	Northeast Utilities	Hartford	±150	-
	Numazu Substation	Japan	+60	IGBT, [23]
2004	Austin Energy	USA	+110/-80	IGBT, 3-level VSI
	Odabizawa	Japan	7/-1	IGBT
2005	Gerdau	USA	+64	VSI
	Voest Alpine	China	+164	VSI
2006	Kalgoorie	Australia	+4	-
2007	Siam Yamato Steel	Thailand	+120	VSI
	Société Nationale des	France	±15	VSI

	Chemins de fer Français			
2008	Asia Special Steel	Japan	+90/-10	VSI
2009	Danieli	Kuwait	+164	VSI
	Danieli	United Arab Emirates	+164	GTO, VSI
	Transelec	Chile	+140/-65	VSI
2010	Concast	Saudi Arabia	+175	VSI
2011	Abul Khair Group	Bangladesh	+110	VSI
	ArcelorMittal	Germany	+48/-32	VSI
	Guangdong Dongguan	China	±640	-
2012	Danieli Far East Co. Ltd	Vietnam	+144	VSI
	Evraz	Canada	+80	VSI
	MGI Steel Factory	Iraq	+164	VSI

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Appendix B Park's Transformation Derivation

Park's transform is a space vector transformation of time-domain signals (i.e., from a stationary *abc*-coordinate system to a rotating *dq*-coordinate system) which has been employed to simplify the analysis of three-phase system. First, the derivation begins by representing the target AC quantities (i.e., grid voltage v_{pcc}) in *abc*-coordinates with a voltage vector v_{pcc} that rotates around the stationary $\alpha\beta$-frame with the angular velocity of ω (i.e., $2\pi f$ at the grid frequency):

$$v_{pcc}\angle\theta^{\circ} = v_{pcc\_a}e^{j0} + v_{pcc\_b}e^{j2\pi/3} + v_{pcc\_c}e^{j4\pi/3} = v_{pcc\_\alpha} + jv_{pcc\_\beta} \tag{B1}$$

where v_{pcc_a}, v_{pcc_b}, and v_{pcc_c} defines the phase vectors for each phase, v_{pcc_α} and v_{pcc_β} defines the projection value of the v_{pcc} onto the stationary $\alpha\beta$ reference frame, and θ is the phase angle of v_{pcc},.

Since $e^{j\sigma} = \cos(\sigma) + j\sin(\sigma)$, (B1) is represented as follows:

$$\begin{aligned} v_{pcc\_\alpha} &= v_{pcc\_a}\cos(0^{\circ}) + v_{pcc\_b}\cos(120^{\circ}) + v_{pcc\_c}\cos(240^{\circ}) \\ &= v_{pcc\_a} - 0.5v_{pcc\_b} - 0.5v_{pcc\_c} \end{aligned} \tag{B2}$$

$$\begin{aligned} v_{pcc\_\beta} &= v_{pcc\_a}\sin(0^{\circ}) + v_{pcc\_b}\sin(120^{\circ}) + v_{pcc\_c}\sin(240^{\circ}) \\ &= +j0.866v_{pcc\_b} - j0.866v_{pcc\_c} \end{aligned} \tag{B3}$$

And can be represented in matrix format as given by:

$$\begin{bmatrix} v_{pcc\_\alpha} \\ v_{pcc\_\beta} \end{bmatrix} = \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & 0.866 & -0.866 \end{bmatrix} \begin{bmatrix} v_{pcc\_a} \\ v_{pcc\_b} \\ v_{pcc\_c} \end{bmatrix} = v_{pcc} \begin{bmatrix} \cos(\theta^{\circ}) \\ \sin(\theta^{\circ}) \end{bmatrix} \tag{B4}$$

The next- and final-step of Park's transformation is to rotate the stationary $\alpha\beta$-coordinates in synchronous with the voltage vector v_{pcc}; thus, making the v_{pcc_α} and v_{pcc_β} to become constant. This transformation matrix is given as follows:

$$\begin{aligned}\begin{bmatrix} v_{pcc\_d} \\ v_{pcc\_q} \end{bmatrix} &= \begin{bmatrix} v_{pcc\_\alpha} \\ v_{pcc\_\beta} \end{bmatrix} \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \\ &= v_{pcc} \begin{bmatrix} \cos(\theta) \\ \sin(\theta) \end{bmatrix} \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \\ &= v_{pcc} \begin{bmatrix} \cos^2(\theta) + \sin^2(\theta) \\ -\sin(\theta)\cos(\theta) + \sin(\theta)\cos(\theta) \end{bmatrix} \\ &= v_{pcc} \begin{bmatrix} 1 \\ 0 \end{bmatrix}\end{aligned} \tag{B5}$$

where v_{pcc_d} and v_{pcc_q} defines the projection of the v_{pcc} onto the rotating *dq* reference frame.

Appendix C Proposed Control Scheme

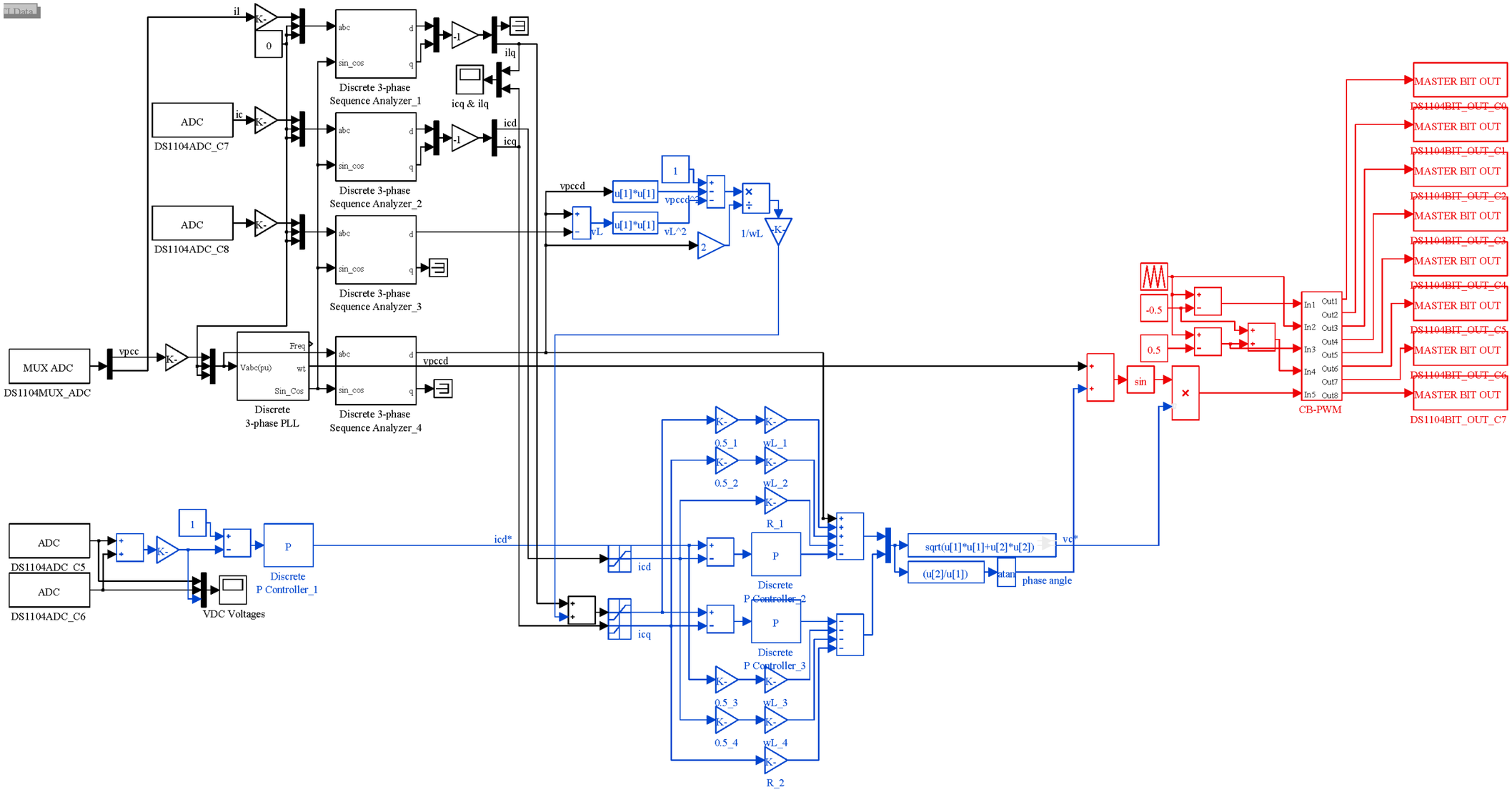

Figure C-1. Model of the proposed control scheme (i.e., blocks in blue) with decoupling current capability and external reactive current reference "i_{cq}^{*} algorithm.

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Appendix D In-Phase Disposition Carrier-Based Pulse Width Modulation

The model of a single-phase five-level CHI with separated DC voltage sources driven by IPD CB-PWM technique is illustrated in Figure D-1. From Figure D-1(a), the "vc" scope block displays the five-level output voltage waveform for m_i = 1 with constant DC voltage-levels as shown in Figure D-1(b)). Figure D-2(a) presents the model of "CB-PWM" block (i.e., red blocks shown in Figure D-1(a)) that generates the dead-band time and switching pattern swapping scheme towards the resultant multipulse trains.

From Figure D-2(a), each "NOT" gate inverts the designated pulse train before feeding it to the specify lower switching device, whereas each "Discrete Edge Detector" block sets a 10 μs turn-on delay for each pulse train to eliminate shoot-through failures. The switching pattern swapping scheme is structured by a collection of blocks (i.e., red blocks shown in Figure D-2(a)) to rotate multipulse trains in a certain sequence over each H-bridge inverter every two cycle (see Figure 2-6). For instance, the "Zero Crossing" block is employed to give a pulse (i.e., trigger event) towards the "Counter" block whenever the resultant sinusoidal STATCOM voltage v_c^* crosses zero (i.e., x-axis line), while each "Switch" block passes through either one of the two designated pulse trains towards a specify switching gate according to the counter value. A full-cycle of resultant multipulse trains captured by the "Switching angles" scope block is illustrated in Figure D-2(b).

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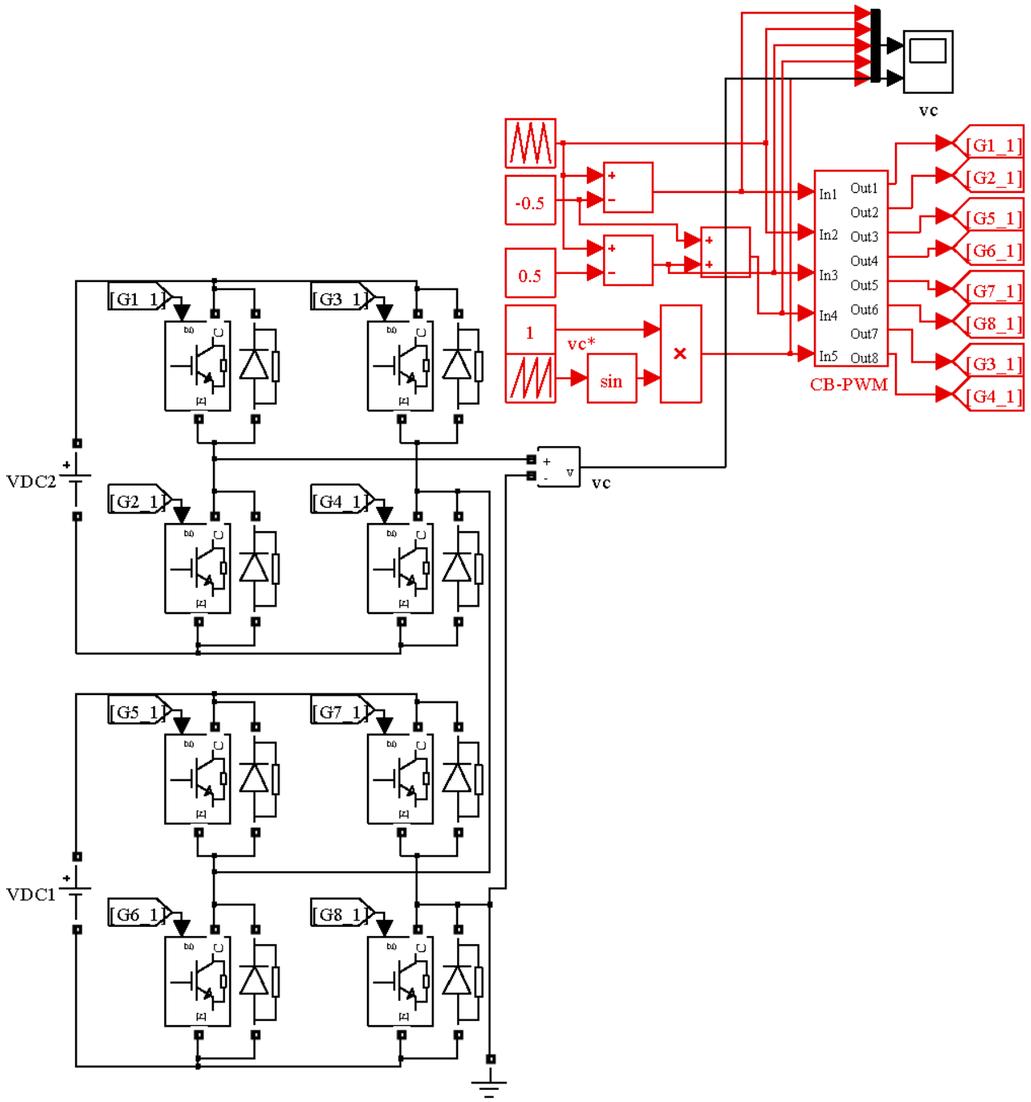
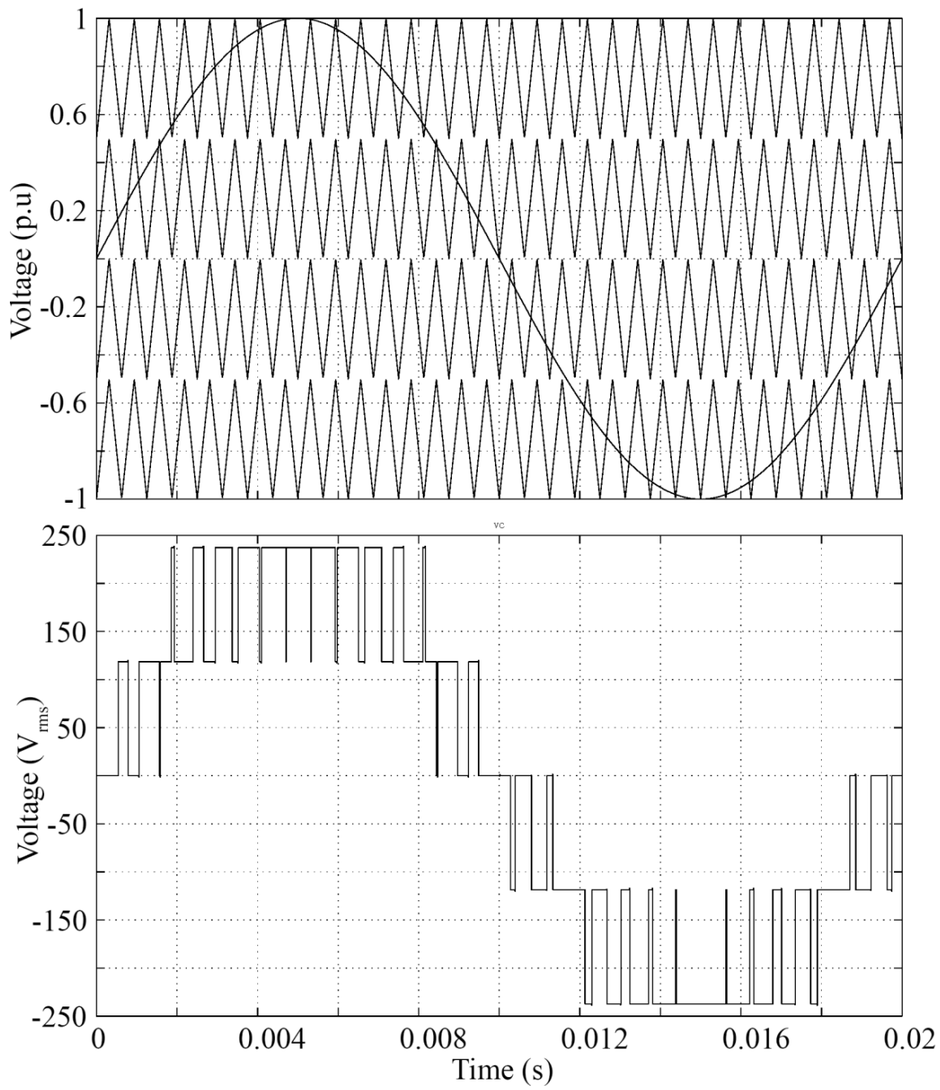
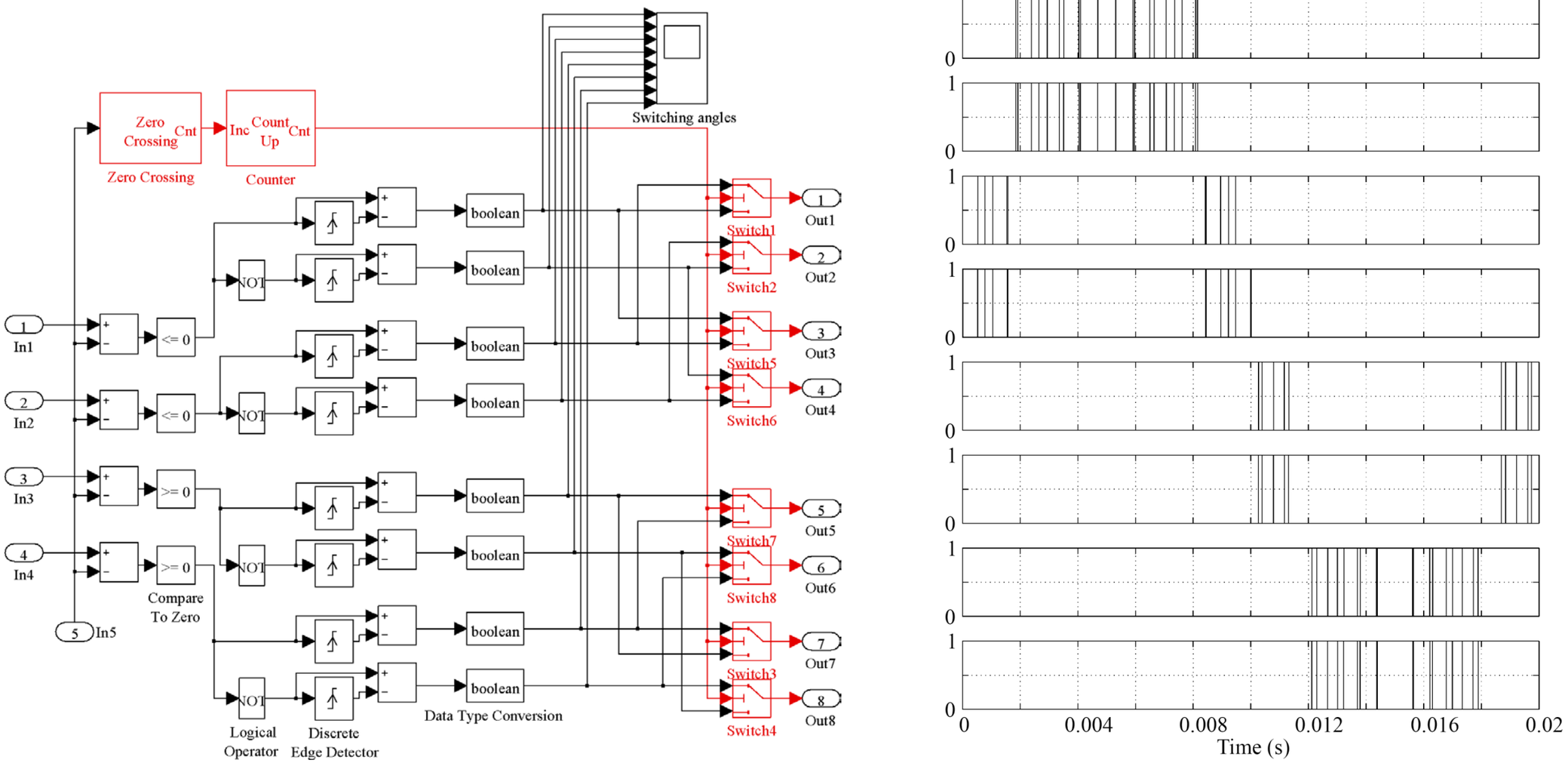


(a)



(b)

Figure D-1. (a) Model of a single-phase five-level CHI with IPD CB-PWM generator block (i.e., blocks in red) and (b) simulation result of five-level voltage waveform generated using IPD CB-PWM technique (i.e., displayed by “vc” scope).



(a) (b)

Figure D-2. (a) Model of the “CB-PWM” block (i.e., red blocks shown in Figure D-1(a)) with switching pattern swapping scheme and (b) simulation result of multipulse trains generated using IPD CB-PWM technique (i.e., displayed by “Switching angles” scope).

Appendix E Five-Level CHI based STATCOM with Separated DC Capacitors, The Associated Proposed Control Scheme, and IPD CB-PWM Technique

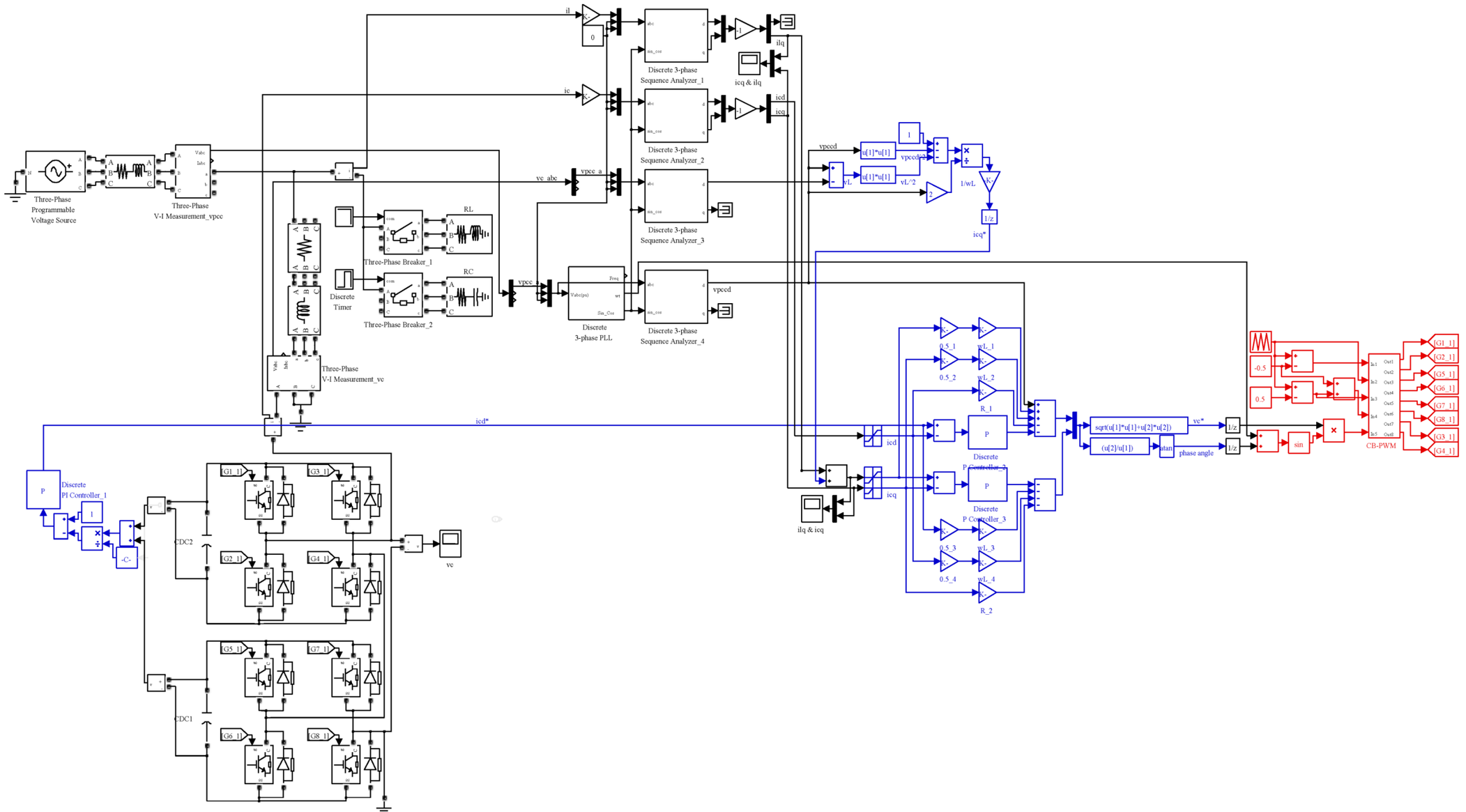


Figure E-1. Model of five-level CHI based single-phase STATCOM with separated DC capacitors and the associated proposed control scheme.

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Appendix F Buck converter

The steady-state operating parameters of the buck converter are given by:

$$\begin{aligned} &V_{SO} = 240\,\text{V}, V_{DC} = D_O V_{SO} = 240 \times 0.25 = 60\,\text{V} \\ &D_O = 0.25,\ f_{sw\_buck} = 2\,\text{kHz}, R_{buck} = 1\Omega, I_{DC} = 60\,\text{A} \end{aligned} \tag{F-1}$$

The size of the inductor L_{buck} and capacitor C_{buck} are defined in (F-2) and (F-3), respectively as follows:

$$L_{buck} = \frac{V_{DC} D_O}{f_{sw\_buck} \Delta I_L} = \frac{V_{DC} D_O}{f_{sw\_buck} I_{DC} D_O} = \frac{60 \times 0.25}{2000 \times 60 \times 0.25} = 0.5x10^{-3}\,\text{H} \tag{F-2}$$

$$C_{buck} = \frac{\frac{1}{2} \times \frac{1}{2 f_{sw\_buck}} \times \frac{I_{DC} D_O}{2}}{\Delta V_{DC}} = \frac{\frac{1}{2} \times \frac{1}{2 \times 2000} \times \frac{60 \times 0.25}{2}}{\frac{60 \times 0.25}{240} \times 60} = 0.25x10^{-3}\,\text{F} \tag{F-3}$$

The cut-off frequency f_{c_buck} of the buck converter represented in both units of Hertz (i.e., Hz) and radians per second (i.e., rad/s) are obtained as follows:

$$f_{c\_buck} = \frac{1}{2\pi\sqrt{L_{buck} C_{buck}}} = \frac{1}{2\pi\sqrt{0.5x10^{-3} \times 0.25x10^{-3}}} = 450.16\,\text{Hz} \tag{F-4}$$

$$\omega_{c\_buck} = \frac{1}{\sqrt{L_{buck} C_{buck}}} = 2828.43 \frac{\text{rad}}{\text{s}} \tag{F-5}$$

The desired closed loop crossover frequency f_{cross_buck}, which determines the bandwidth of the buck converter, is chosen to be two times higher than the cut-off frequency as given by:

$$f_{cross\_buck} = 2 f_{c\_buck} = 900.32\,\text{Hz} \tag{F-6}$$

$$\omega_{cross\_buck} = 2\pi f_{cross\_buck} = 5656.85 \frac{\text{rad}}{\text{s}} \tag{F-7}$$

Based on the defined buck converter's transfer function $G_{conv}(s)$ (see (4-20)), the frequency response of the buck converter at crossover frequency is given as follows:

$$s = j\omega_{cross\_buck} \tag{F-8}$$

$$\begin{aligned} G_{conv}\left(j\omega_{cross\_buck}\right) &= \frac{v_{DC}\left(j\omega_{cross\_buck}\right)}{d\left(j\omega_{cross\_buck}\right)} \\ &= \frac{V_{SO}}{\left(j\omega_{cross\_buck}\right)^2 L_{buck}C_{buck} + \frac{j\omega_{cross\_buck}\times L_{buck}}{R_{buck}} + 1} \\ &= \frac{240}{-\left(5656.85\right)^2 \times \left(0.5x10^{-3}\times 0.25x10^{-3}\right) + j\left(5656.85\times 0.5x10^{-3}\right)+1} \\ &= \frac{240}{-3+j11.31} = \frac{240}{11.70\angle 104.85^\circ} = 20.51\angle -104.85^\circ \\ &= G_{conv\_mag}\angle G_{conv\_\text{phase}}{}^\circ \end{aligned} \tag{F-9}$$

In [187], the Phase Margin (PM) of 60° (see (F-10)) is suggested to achieve a good compromise between fast transient response and stability (i.e., less PM = less damping) of the closed loop response.

$$\text{PM} = 180^\circ + G_{conv\_phase} = 60^\circ \tag{F-10}$$

Besides that, the amount Phase Boost (PB) required from the zero-pole pair in the error amplifier (see (4-21)) is given by:

$$\begin{aligned} \text{PB} &= \text{PM} - 180^\circ - G_{conv\_phase} + 90^\circ \\ &= 60^\circ - 180^\circ - \left(-104.85^\circ\right) + 90^\circ = 74.85^\circ \end{aligned} \tag{F-11}$$

Equation (F-12) relates the K factor to the amount of PB required from the error amplifier to achieve the desired PM.

$$K = \tan\left(\frac{\text{PB}}{2} + 45^\circ\right) = \tan\left(\frac{74.85^\circ}{2} + 45^\circ\right) = 7.52 \tag{F-12}$$

By substituting (F-12) into (4-21), the zero- ω_{z_buck} and pole-frequency ω_{p_buck} are obtained as follows:

$$\omega_{z\_buck} = \frac{\omega_{cross\_buck}}{K} = \frac{5656.85}{7.52} = 752.24\frac{\text{rad}}{\text{s}} \tag{F-13}$$

$$\omega_{p\_buck} = \omega_{cross\_buck} \times K = 5656.85 \times 7.52 = 42539.51 \frac{\text{rad}}{\text{s}} \tag{F-14}$$

Finally, (F-7), (F-13), and (F-14) are added into (4-21) to obtain the desired gain *A* of the error amplifier as follows:

$$\begin{aligned} \left|G_v\left(j\omega_{cross\_buck}\right)\right| &= \frac{A}{\left|j\omega_{cross\_buck}\right|}\left[\frac{\sqrt{1^2+\left(\frac{j\omega_{cross\_buck}}{\omega_z}\right)^2}}{\sqrt{1^2+\left(\frac{j\omega_{cross\_buck}}{\omega_p}\right)^2}}\right] \\ &= \frac{A}{\left|5656.85\right|}\left[\frac{\sqrt{1^2+\left(-7.52\right)^2}}{\sqrt{1^2+\left(-0.13\right)^2}}\right] \\ &= \frac{A}{5656.85}\left[\frac{7.59}{1.01}\right] = A \times 1.33x10^{-3} \end{aligned} \tag{F-15}$$

$$\begin{aligned} \left|G_{conv}\left(j\omega_{cross\_buck}\right)\right|\left|G_v\left(j\omega_{cross\_buck}\right)\right| &= 1 \\ \left(20.51\right)\times\left(A \times 1.33x10^{-3}\right) &= 1 \end{aligned} \tag{F-16}$$

$$A = \frac{1}{20.51 \times 1.33x10^{-3}} = 36.66 \tag{F-17}$$

The transfer function of the error amplifier $G_v(s)$ (see (4-21)) is defined as:

$$\begin{aligned} G_v\left(s\right) &= \frac{A}{s}\left[\frac{1+\frac{s}{\omega_{z\_buck}}}{1+\frac{s}{\omega_{p\_buck}}}\right] = \frac{36.66}{s}\left[\frac{1+\frac{s}{752.24}}{1+\frac{s}{42539.51}}\right] \\ &= \frac{36.66}{s}\left[\frac{1+1.33x10^{-3}s}{1+23.51x10^{-6}s}\right] \end{aligned} \tag{F-18}$$

Figure F-1 illustrates the model of the voltage mode closed loop controller of DC-DC buck converter which is represented by (F-18). The dynamic and transient responses of the buck converter voltage tracking characteristics in response to the step changes of reference output voltage (i.e., 50 V, 100 V, and 150 V) is presented in Figure F-2.

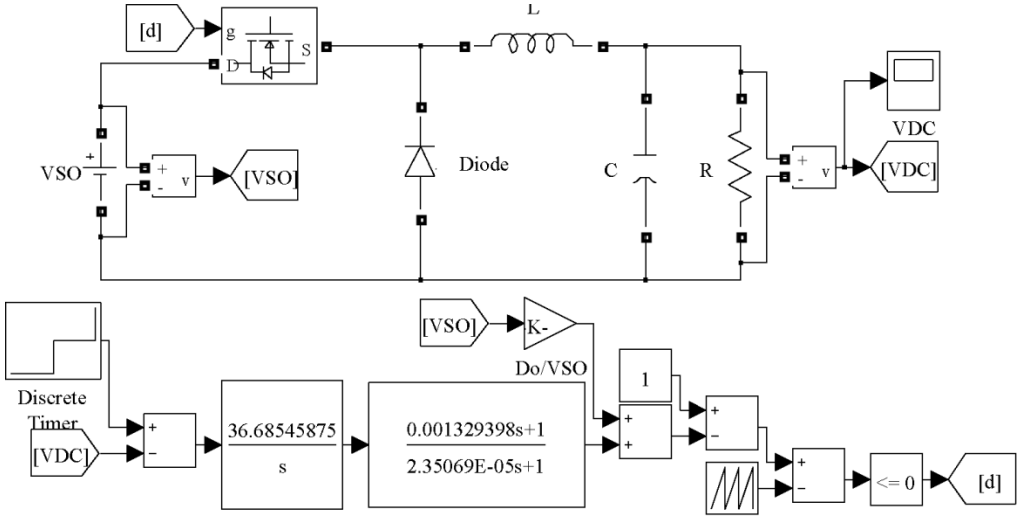

Figure F-1. Model of DC-DC buck converter with the associated voltage mode closed loop controller.

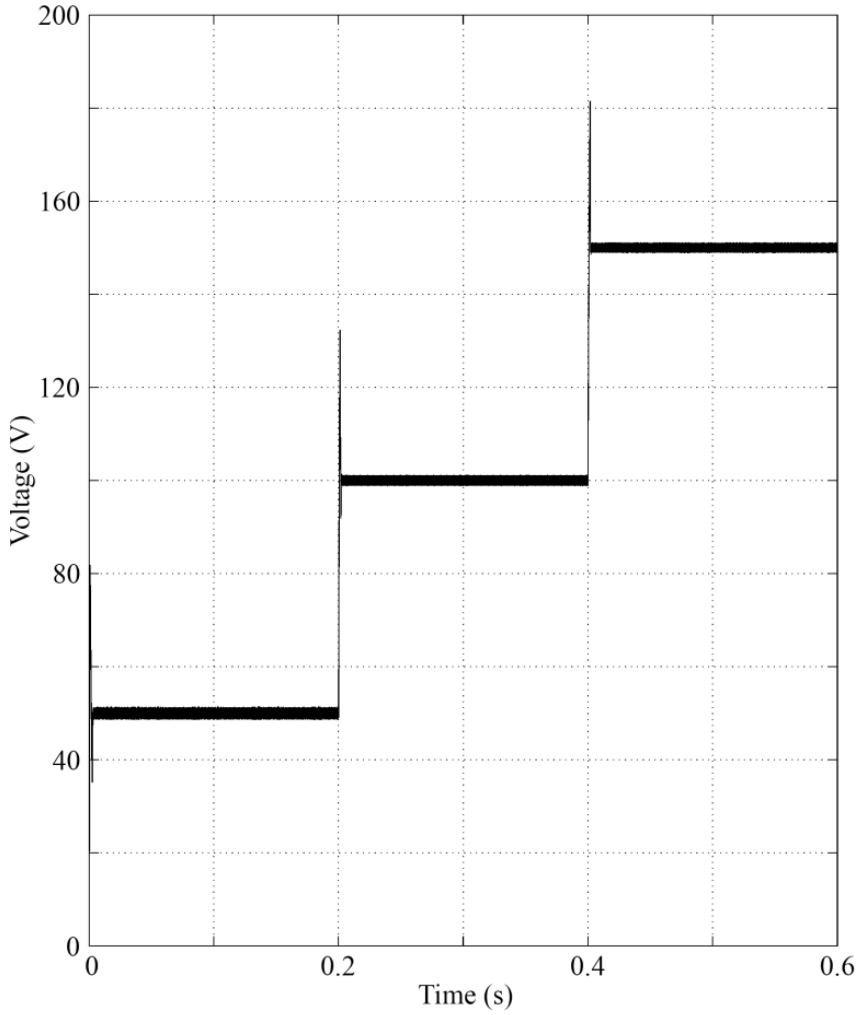

Figure F-2. Simulation results of step changes in the reference output voltage (i.e., displayed by “VDC” scope).

Appendix G MSHE-PWM *N* = 3/5 with Variable DC Voltage-Levels

The model of a single-phase five-level CHI with separated DC-DC buck converters driven by MSHE-PWM with variable DC voltage-levels technique is illustrated in Figure G-2. From Figure G-2(a), the "vc" scope block displays the five-level output voltage waveform for m_i = 1 with variable DC voltage-levels as shown in Figure G-2(b). Figure G-3 presents the model of "MSHE-PWM 3/5" block (i.e., red blocks shown in Figure G-2(a)) that generates the dead-band time towards the resultant multipulse trains.

From Figure G-3(a), each "Discrete Edge Detector" block sets a 10 μs turn-on delay for each pulse train to eliminate shoot-through failures, whereas Figure G-3(b) illustrates a full-cycle of resultant multipulse trains captured by the "Switching angles" scope block.

Figure G-4 shows the implemented model of "MSHE-PWM 3/5 with variable DC voltage-levels" block (i.e., red blocks shown in Figure G-3(a)), which generates the MSHE-PWM pulse trains according to the switching angles that are stored in the "lookup table (2-D)" block. The concept of generating the MSHE-PWM pulse train via the XOR gates is illustrated in Figure G-1 below:

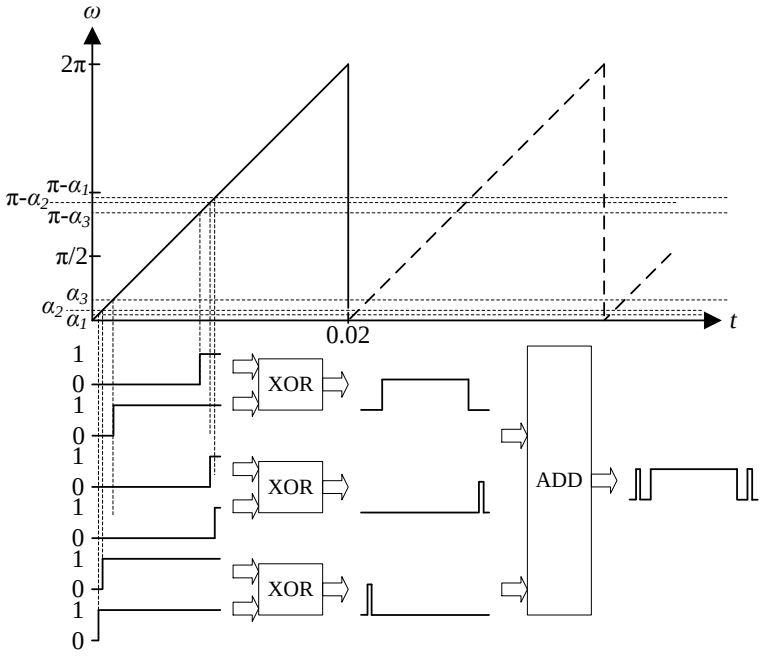

Figure G-1. Concept of generating MSHE-PWM between zero- and the first-level.

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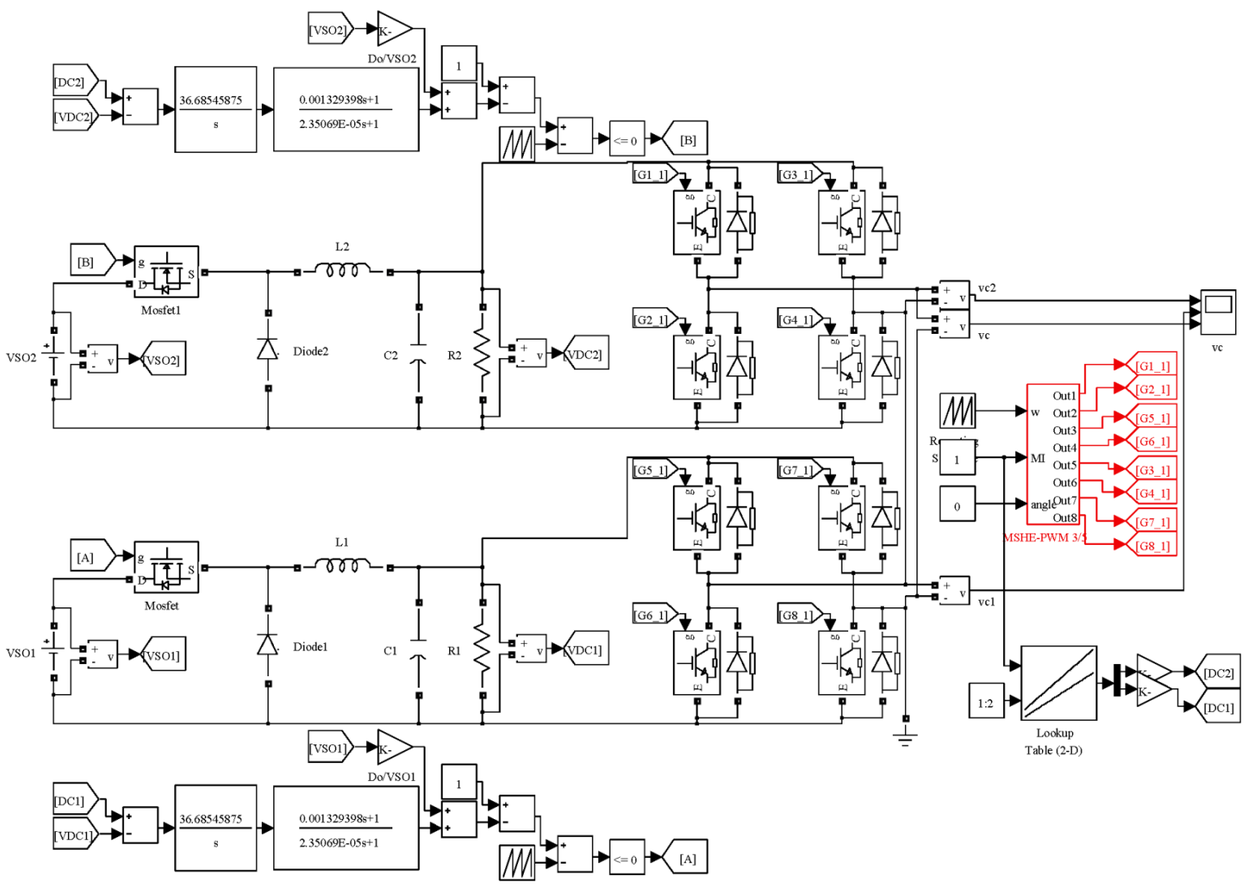
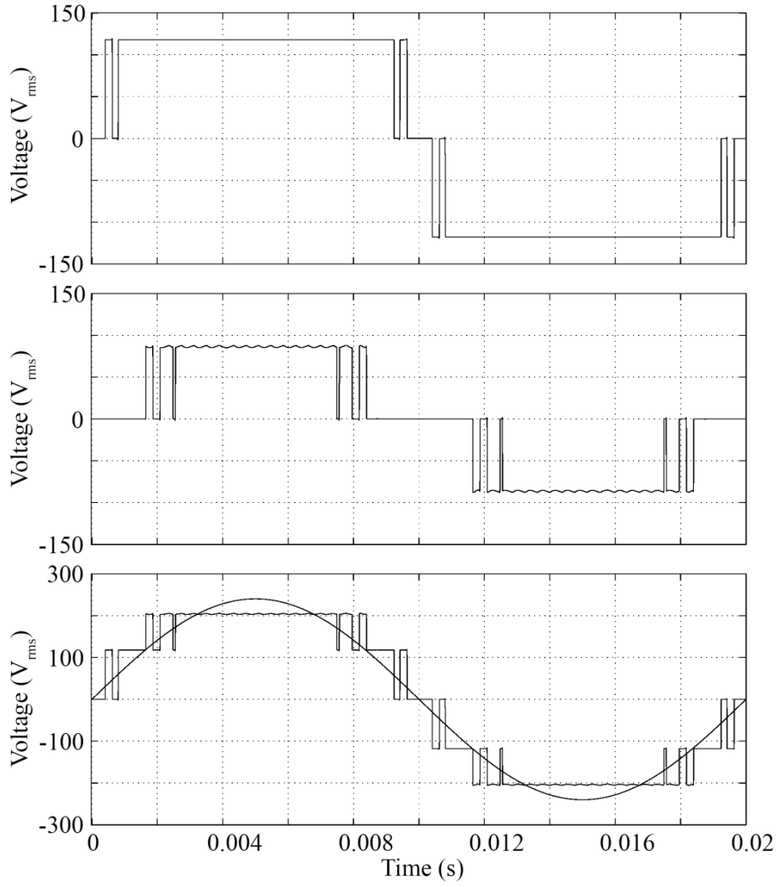
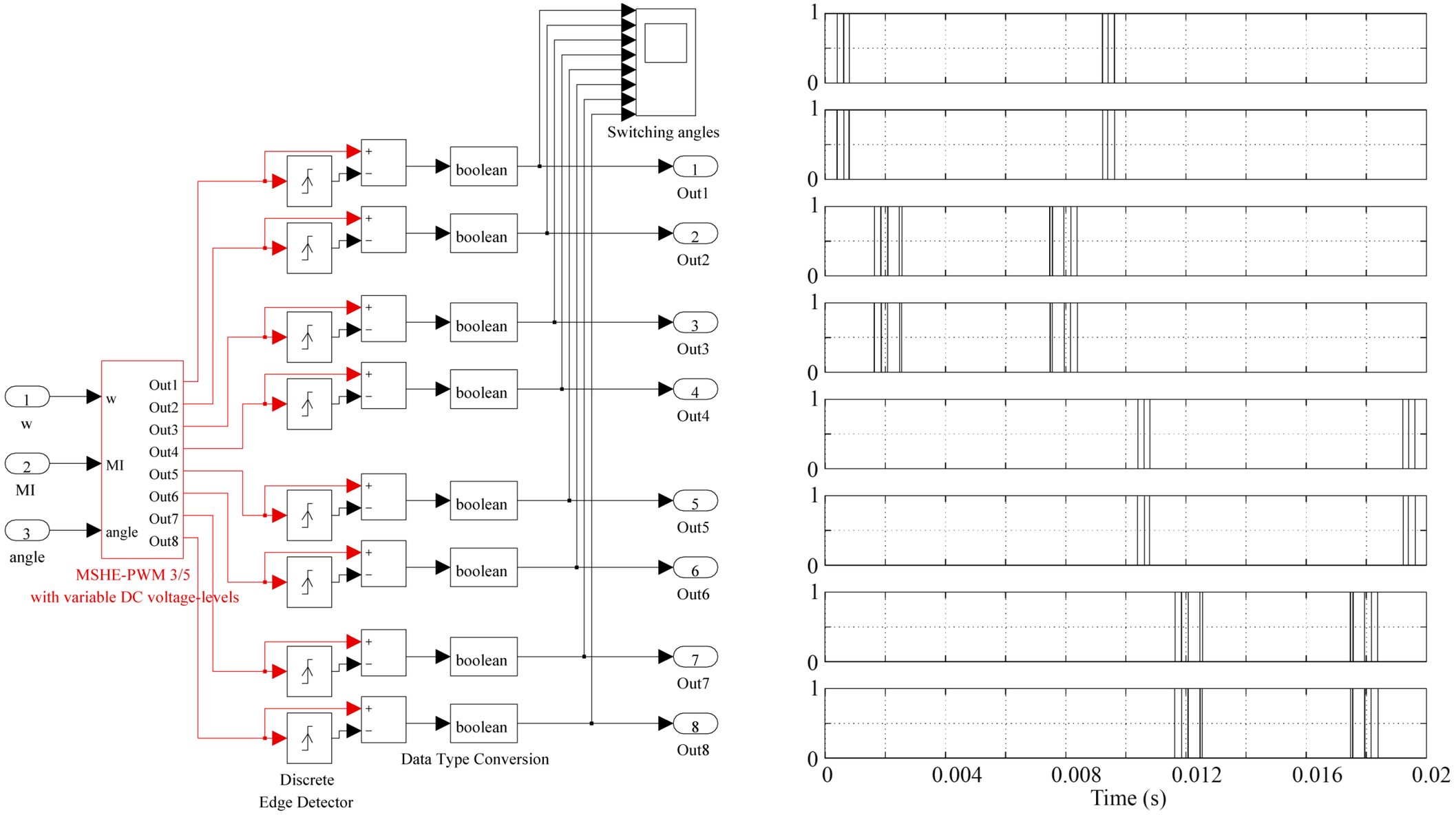


(a)



(b)

Figure G-2. (a) Model of a single-phase five-level CHI with MSHE-PWM generator block (i.e., blocks in red) and (b) simulation result of five-level voltage waveform generated using MSHE-PWM 3/5 with variable DC voltage-levels technique (i.e., displayed by “vc” scope).



(a) (b)

Figure G-3. (a) Model of the “MSHE-PWM 3/5” block (i.e., red blocks shown in Figure G-2(a)) and (b) simulation result of multipulse trains generated using MSHE-PWM with variable DC voltage-levels technique (i.e., displayed by “Switching angles” scope).

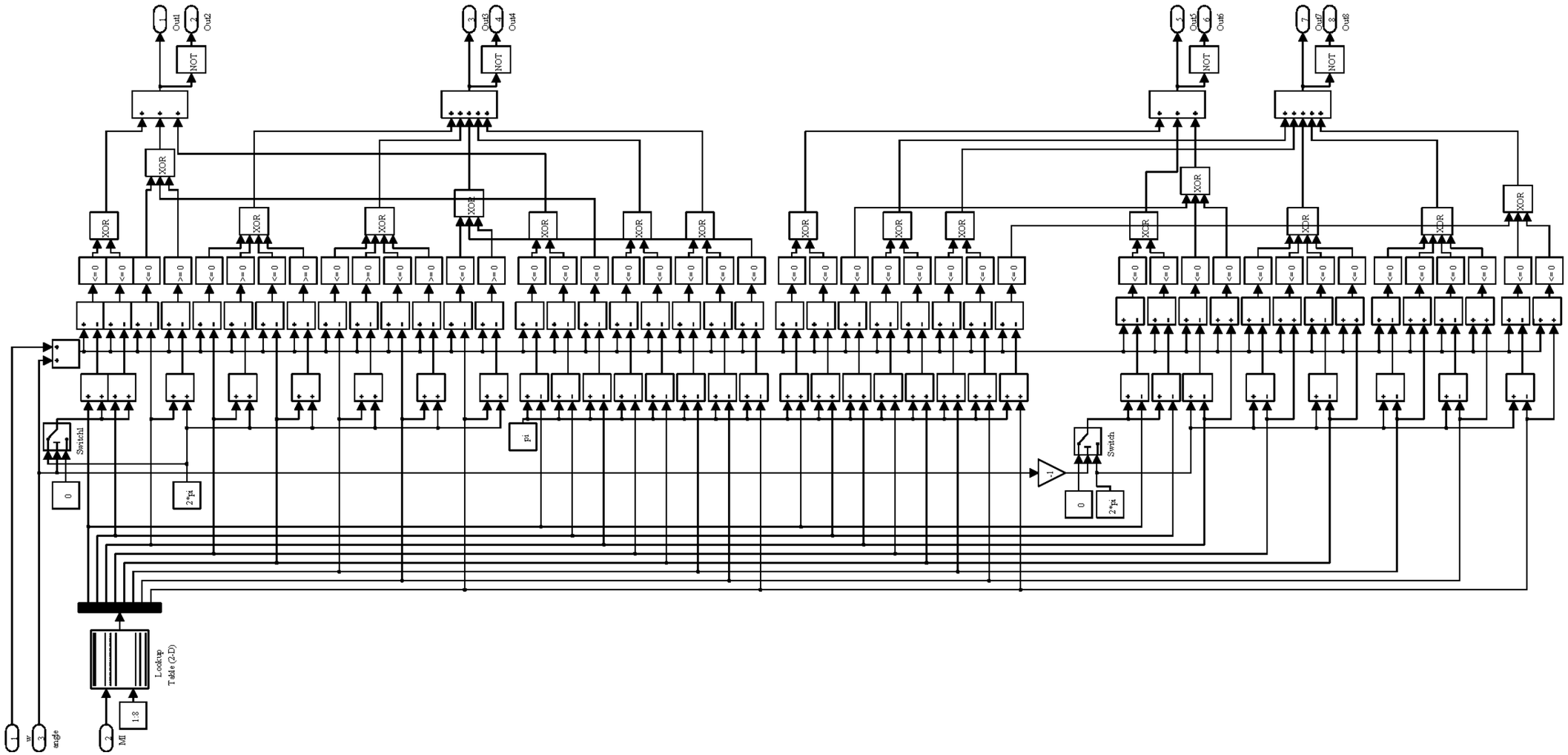


Figure G-4. Model of the “MSHE-PWM 3/5 with variable DC voltage-levels” block (i.e., red blocks shown in Figure G-3(a)).

Appendix H Five-Level CHI based STATCOM with Separated DC Voltage Sources, The Associated Proposed Control Scheme, and IPD CB-PWM Technique

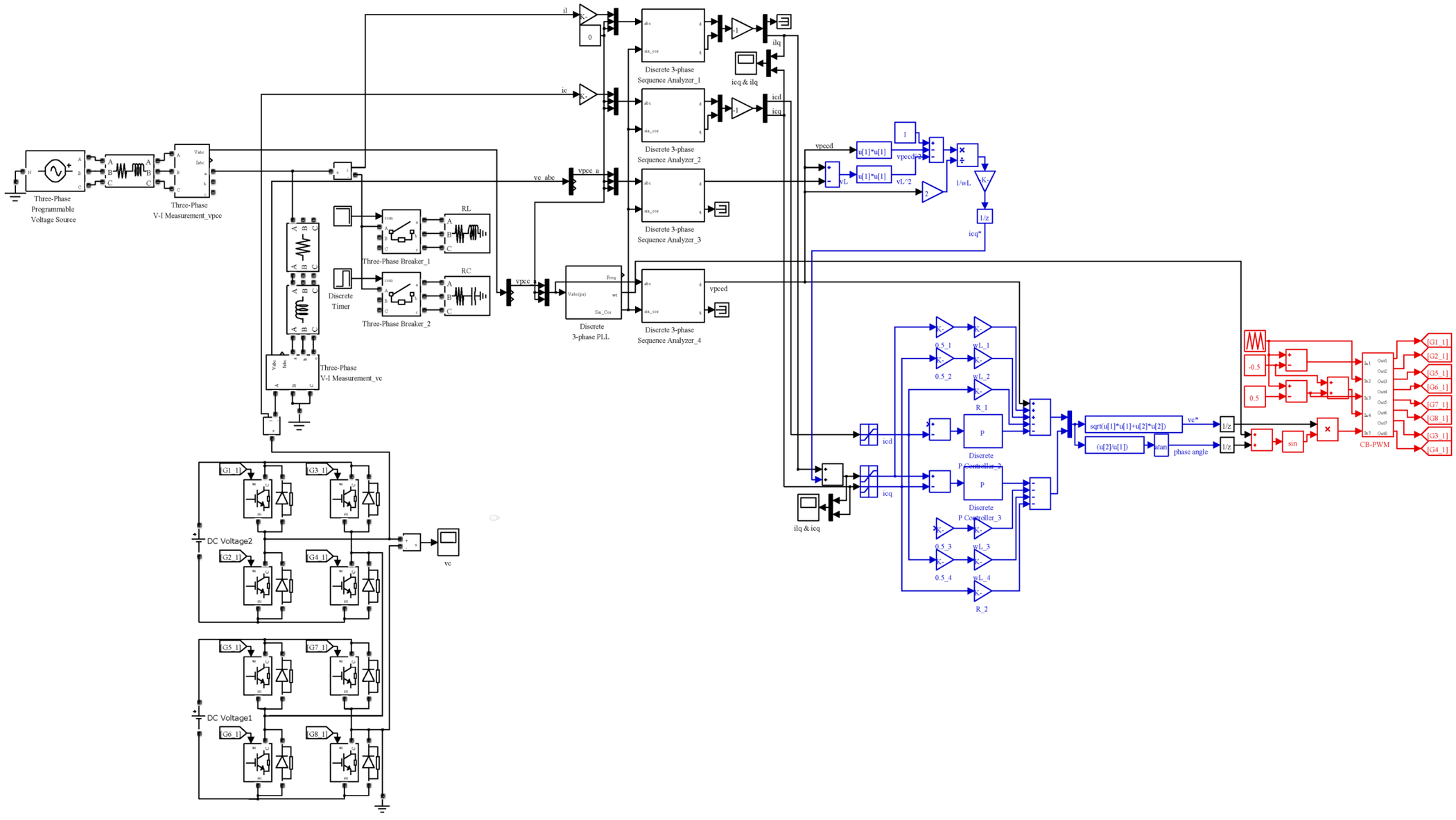


Figure H-1. Model of five-level CHI based single-phase STATCOM with separated DC voltage sources and the associated proposed control scheme.

Appendix I Five-Level CHI based STATCOM with The Associated Proposed Control Scheme and MSHE-PWM N = 3/5 with Variable DC Voltage-Levels Technique

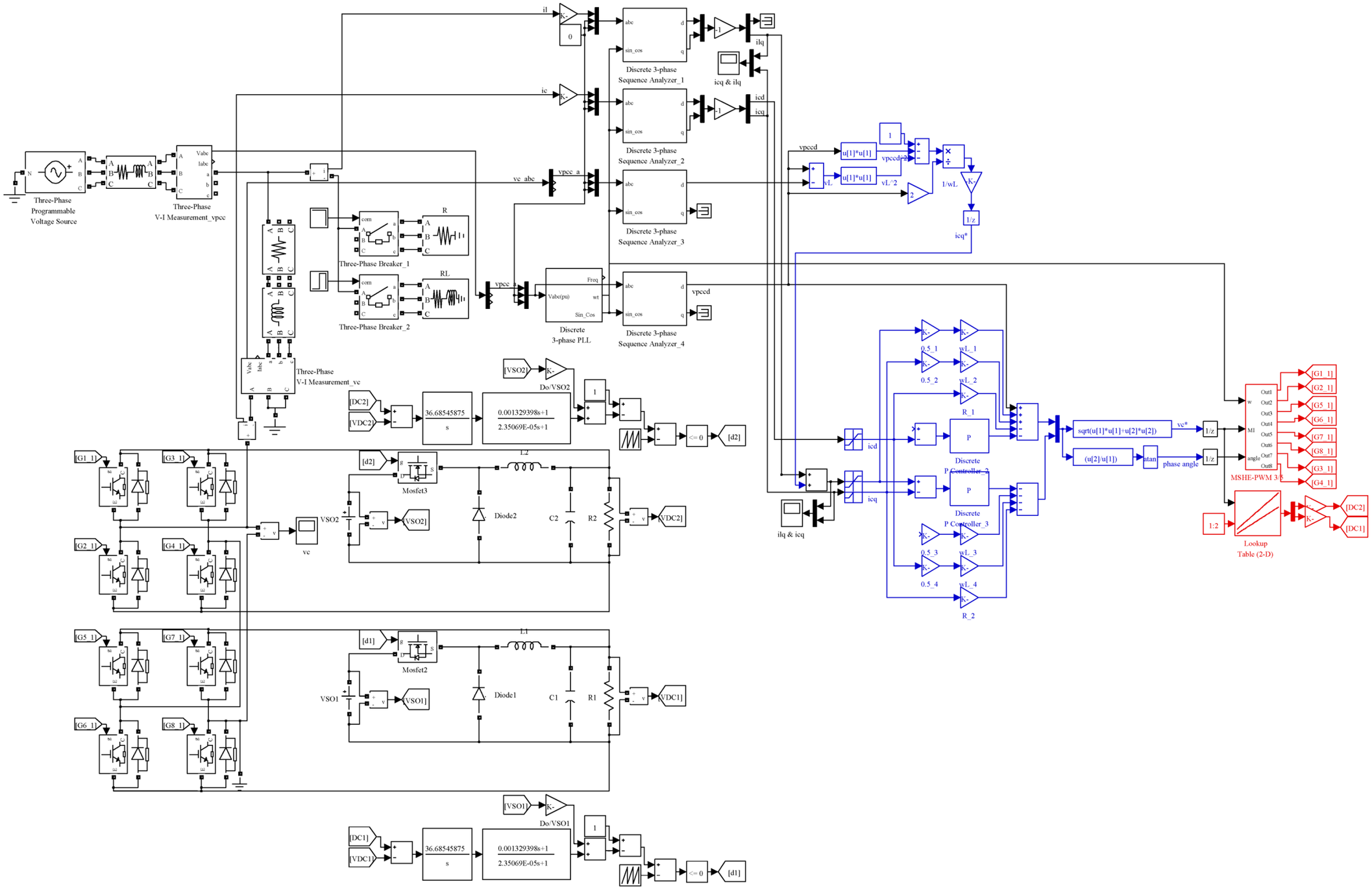


Figure I-1. Model of five-level CHI based single-phase STATCOM controlled by the associated proposed control scheme and MSHE-PWM 3/5 with variable DC voltage-levels technique.

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Appendix J Boost converter

The steady-state operating parameters of the boost converter are given by:

$$V_{SO} = 60\,\text{V}, V_{DC} = \frac{V_{SO}}{1-D_O} = \frac{60}{0.4} = 150\,\text{V}$$
$$D_O = 0.6,\ f_{sw\_boost} = 25\,\text{kHz}, R_{boost} = 10\,\Omega, I_{DC} = 15\,\text{A} \tag{J-1}$$

The size of the inductor L_{boost} and capacitor C_{boost} are defined in (J-2) and (J-3), respectively as follows:

$$L_{boost} = \frac{V_{SO}D_O}{f_{sw\_boost}\Delta I_L} = \frac{V_{SO}D_O}{f_{sw\_boost}\frac{I_{DC}}{1-D_O}D_O} = \frac{60\times 0.6}{25000\times\frac{15}{0.4}\times 0.6} = 6.4x10^{-6}\,\text{H} \tag{J-2}$$

$$C_{boost} = \frac{\frac{1}{2}\times\frac{1}{2f_{sw\_boost}}\times\frac{I_{DC}}{2(1-D_O)}}{\Delta V_{DC}} = \frac{\frac{1}{2}\times\frac{1}{2\times 25000}\times\frac{15}{2\times 0.4}}{\frac{15}{60\times 0.4}} = 300x10^{-6}\,\text{F} \tag{J-3}$$

The cut-off frequency f_{c_boost} of the boost converter represented in both units of Hertz (i.e., Hz) and radians per second (i.e., rad/s) are obtained as follows:

$$f_{c\_boost} = \frac{1}{2\pi\sqrt{L_{boost}C_{boost}}} = \frac{1}{2\pi\sqrt{6.4x10^{-6}\times 300x10^{-6}}} = 3632.20\,\text{Hz} \tag{J-4}$$

$$\omega_{c\_boost} = \frac{1}{\sqrt{L_{boost}C_{boost}}} = 22822\frac{\text{rad}}{\text{s}} \tag{J-5}$$

The desired closed loop crossover frequency f_{cross_boost}, which determines the bandwidth of the boost converter, is chosen to be one half of the cut-off frequency due to the right-half plane zero (see (4-33)) as given by:

$$f_{cross\_boost} = \frac{f_{c\_boost}}{2} = 1816.10\,\text{Hz} \tag{J-6}$$

$$\omega_{cross\_boost} = \frac{2\pi f_{cross\_boost}}{2} = 11411\frac{\text{rad}}{\text{s}} \tag{J-7}$$

Based on the defined boost converter's transfer function $G_{conv}(s)$ (see (4-33)), the frequency response of the boost converter at crossover frequency is given as follows:

$$s = j\omega_{cross\_boost} \tag{J-8}$$

$$\begin{aligned} G_{conv}\left(j\omega_{cross\_boost}\right) &= \frac{v_{DC}\left(j\omega_{cross\_boost}\right)}{d\left(j\omega_{cross\_boost}\right)} \\ &= \frac{\left(\frac{V_{SO}}{(1-D_O)^2}\left(1-\frac{j\omega_{cross\_boost}\times L_{boost}}{(1-D_O)^2 R_{boost}}\right)\right)}{\frac{\left(j\omega_{cross\_boost}\right)^2 L_{boost}C_{boost}}{(1-D_O)^2}+\frac{j\omega_{cross\_boost}\times L_{boost}}{(1-D_O)^2 R_{boost}}+1} \\ &= \frac{\left(\frac{60}{(1-0.6)^2}\left(1-\frac{j11411\times 6.4x10^{-6}}{(1-0.6)^2\times 10}\right)\right)}{\frac{\left(j11411\right)^2\times 6.4x10^{-6}\times 300x10^{-6}}{(1-0.6)^2}+\frac{j11411\times 6.4x10^{-6}}{(1-0.6)^2\times 10}+1} \\ &= \frac{375\left(1-j0.0456\right)}{-0.56+j0.0456} = \frac{375\angle -2.61^\circ}{0.56\angle 175.34^\circ} = 670.34\angle -177.95^\circ \\ &= G_{conv\_mag}\angle G_{conv\_\text{phase}}{}^\circ \end{aligned} \tag{J-9}$$

In [187], the Phase Margin (PM) of 70° (see (J-10)) is suggested to achieve a good compromise between fast transient response and stability (i.e., less PM = less damping) of the closed loop response.

$$\text{PM} = 270^\circ + G_{conv\_phase} = 70^\circ \tag{J-10}$$

Besides that, the amount PB required from the zero-pole pair in the error amplifier (see (4-34)) is given by:

$$\begin{aligned} \text{PB} &= \text{PM} - 270^\circ - G_{conv\_phase} + 90^\circ \\ &= 70^\circ - 270^\circ - \left(-177.95^\circ\right) + 90^\circ = 67.95^\circ \end{aligned} \tag{J-11}$$

Equation (J-12) relates the K factor to the amount of PB required from the error amplifier to achieve the desired PM.

$$K=\tan\left(\frac{\mathrm{PB}}{2}+45^{\circ}\right)=\tan\left(\frac{67.95^{\circ}}{2}+45^{\circ}\right)=5.13 \tag{J-12}$$

By substituting (J-12) into (4-34), the zero- ω_{z_boost} and pole-frequency ω_{p_boost} are obtained as follows:

$$\omega_{z\_boost}=\frac{\omega_{cross\_boost}}{K}=\frac{11411}{5.13}=2224.37\frac{\mathrm{rad}}{\mathrm{s}} \tag{J-13}$$

$$\omega_{p\_boost}=\omega_{cross\_boost}\times K=11411\times 5.13=58538.43\frac{\mathrm{rad}}{\mathrm{s}} \tag{J-14}$$

Finally, (J-7), (J-13), and (J-14) are added into (4-34) to obtain the desired gain A of the error amplifier as follows:

$$\begin{aligned}\left|G_v\left(j\omega_{cross\_boost}\right)\right| &= \frac{A}{\left|j\omega_{cross\_boost}\right|}\left[\frac{\sqrt{1^2+\left(\frac{j\omega_{cross\_boost}}{\omega_z}\right)^2}}{\sqrt{1^2+\left(\frac{j\omega_{cross\_boost}}{\omega_p}\right)^2}}\right]\\ &= \frac{A}{|11411|}\left[\frac{\sqrt{1^2+(-5.13)^2}}{\sqrt{1^2+(-0.195)^2}}\right]\\ &= \frac{A}{11411}\left[\frac{5.23}{1.02}\right]=A\times 0.45x10^{-3}\end{aligned} \tag{J-15}$$

$$\begin{aligned}\left|G_{conv}\left(j\omega_{cross\_boost}\right)\right|\left|G_v\left(j\omega_{cross\_boost}\right)\right| &= 1\\ (670.34)\times\left(A\times 0.45x10^{-3}\right) &= 1\end{aligned} \tag{J-16}$$

$$A=\frac{1}{670.34\times 0.45x10^{-3}}=3.32 \tag{J-17}$$

The transfer function of the error amplifier $G_v(s)$ (see (4-34)) is defined as:

$$G_v(s)=\frac{A}{s}\left[\frac{1+\frac{s}{\omega_{z\_buck}}}{1+\frac{s}{\omega_{p\_buck}}}\right]=\frac{3.32}{s}\left[\frac{1+\frac{s}{2224.37}}{1+\frac{s}{58538.43}}\right]=\frac{3.32}{s}\left[\frac{1+0.45x10^{-3}s}{1+17.1x10^{-6}s}\right] \tag{J-18}$$

Figure J-1 illustrates the model of the voltage mode closed loop controller of DC-DC boost converter which is represented by (J-18).

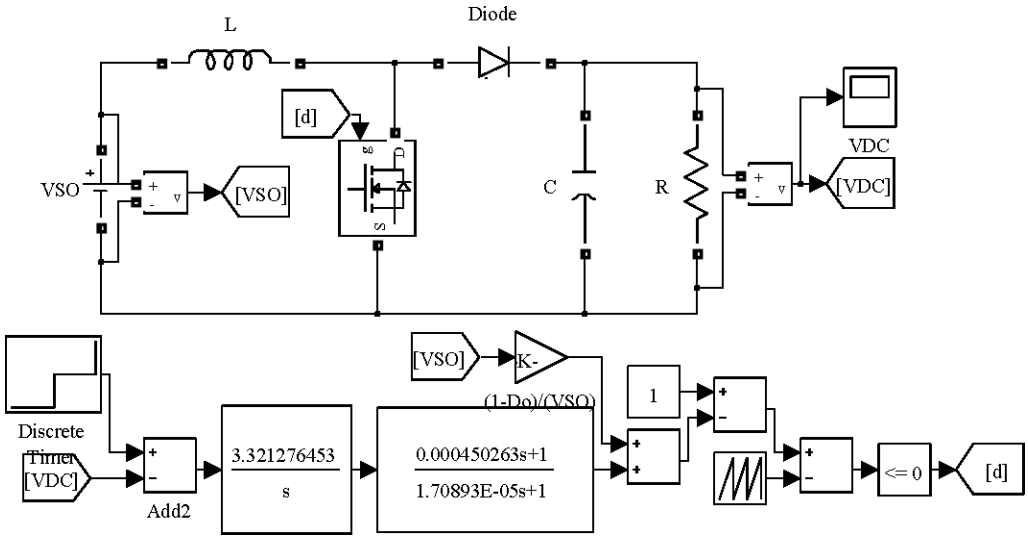

Figure J-1. Model of DC-DC boost converter with the associated voltage mode closed loop controller.

The dynamic and transient responses of the boost converter voltage tracking characteristics in response to the step changes of reference output voltage (i.e., 50 V, 100 V, and 150 V) is presented in Figure J-2.

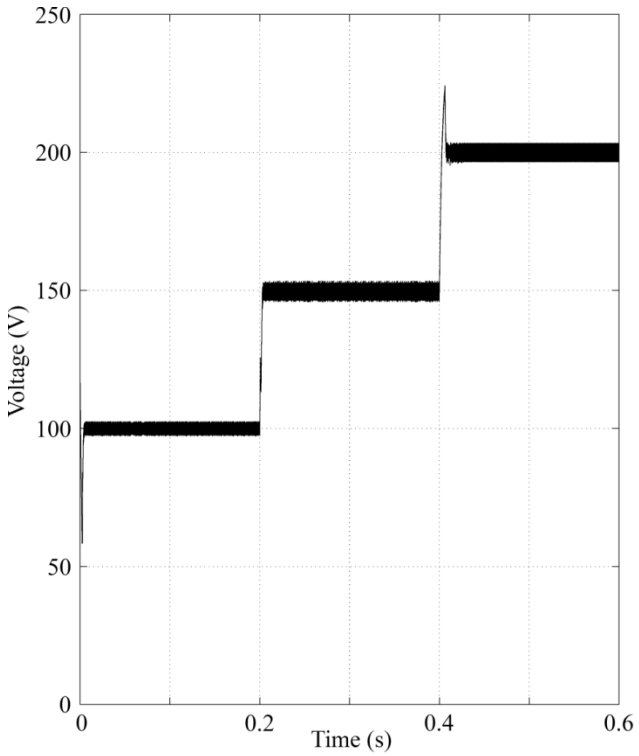

Figure J-2. Simulation results of step changes in the reference output voltage (i.e., displayed by “VDC” scope).

Appendix K MSHE-PWM N = 3/8 with Variable DC Voltage-Levels

The model of a single-phase five-level CHI with separated DC-DC boost converters driven by MSHE-PWM with variable DC voltage-levels technique is illustrated in Figure K-1. From Figure K-1(a), the "vc" scope block displays the five-level output voltage waveform for m_i = 1 with variable DC voltage-levels as shown in Figure K-1(b). Figure K-2 presents the model of "MSHE-PWM 3/8" block (i.e., red blocks shown in Figure K-1(a)) that generates the dead-band time towards the resultant multipulse trains.

From Figure K-2(a), each "Discrete Edge Detector" block sets a 10 μs turn-on delay for each pulse train to eliminate shoot-through failures, whereas Figure K-2(b) illustrates a full-cycle of resultant multipulse trains captured by the "Switching angles" scope block.

Figure K-3 shows the implemented model of "MSHE-PWM 3/8 with variable DC voltage-levels" block (i.e., red blocks shown in Figure K-2(a)), which generates the MSHE-PWM pulse trains according to the switching angles that are stored in the "lookup table (2-D)" block. The concept of generating the MSHE-PWM pulse train via the XOR gates is illustrated in Appendix G (see Figure G-1).

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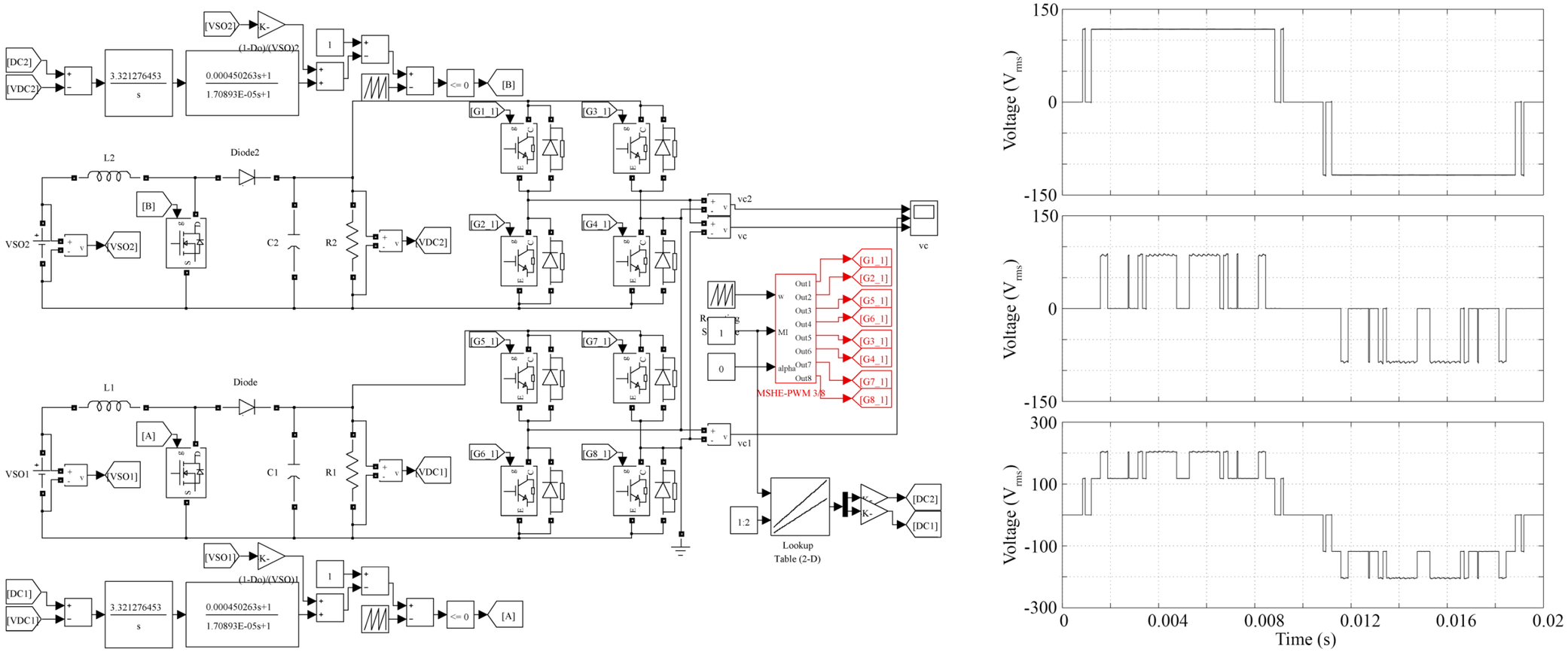
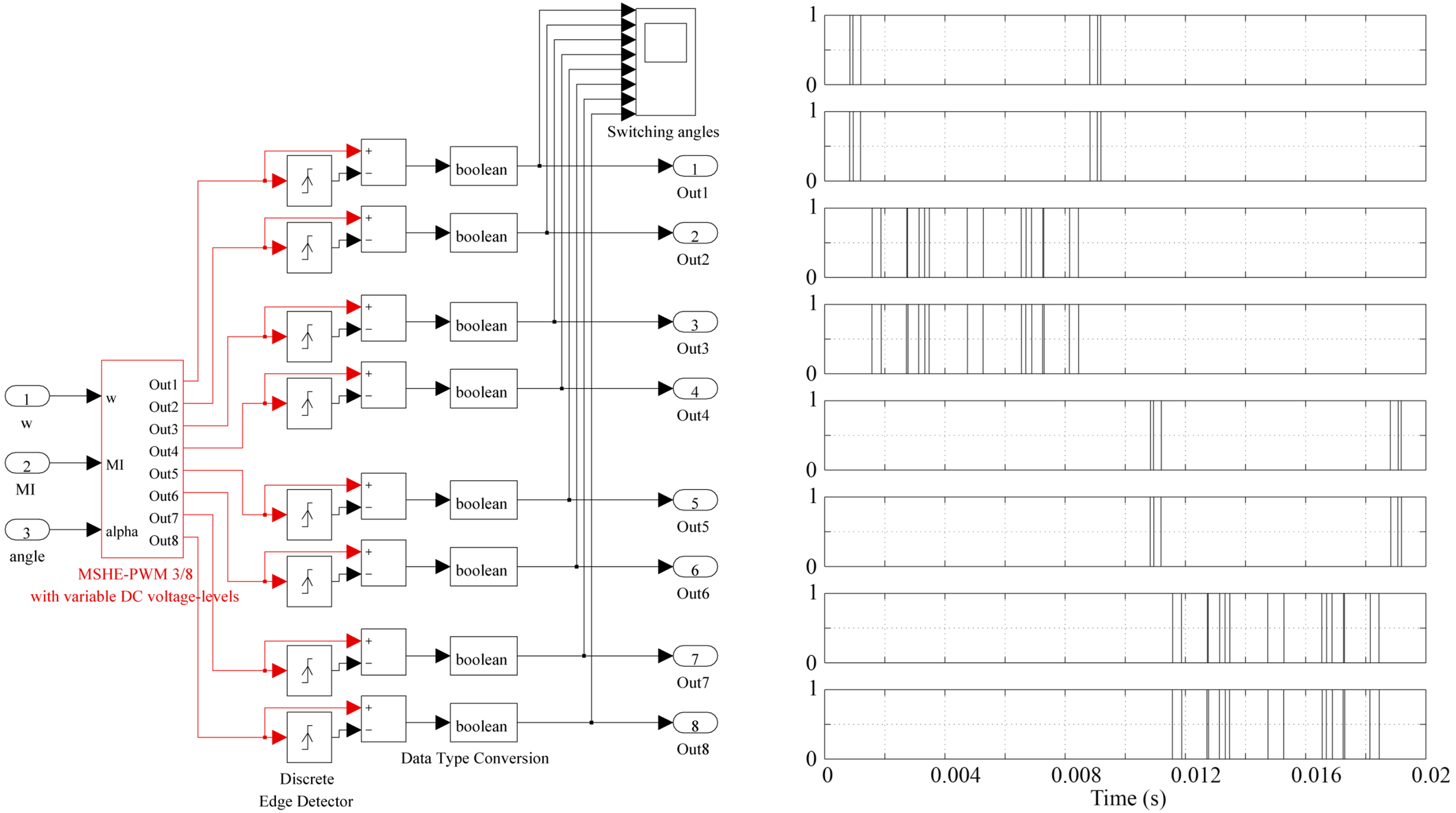


(a) (b)

Figure K-1. (a) Model of a single-phase five-level CHI with MSHE-PWM generator block (i.e., blocks in red) and (b) simulation result of five-level voltage waveform generated using MSHE-PWM 3/8 with variable DC voltage-levels technique (i.e., displayed by “vc” scope).



(a) (b)

Figure K-2. (a) Model of the “MSHE-PWM 3/8” block (i.e., red blocks shown in Figure K-1(a)) and (b) simulation result of multipulse trains generated using MSHE-PWM with variable DC voltage-levels technique (i.e., displayed by “Switching angles” scope).

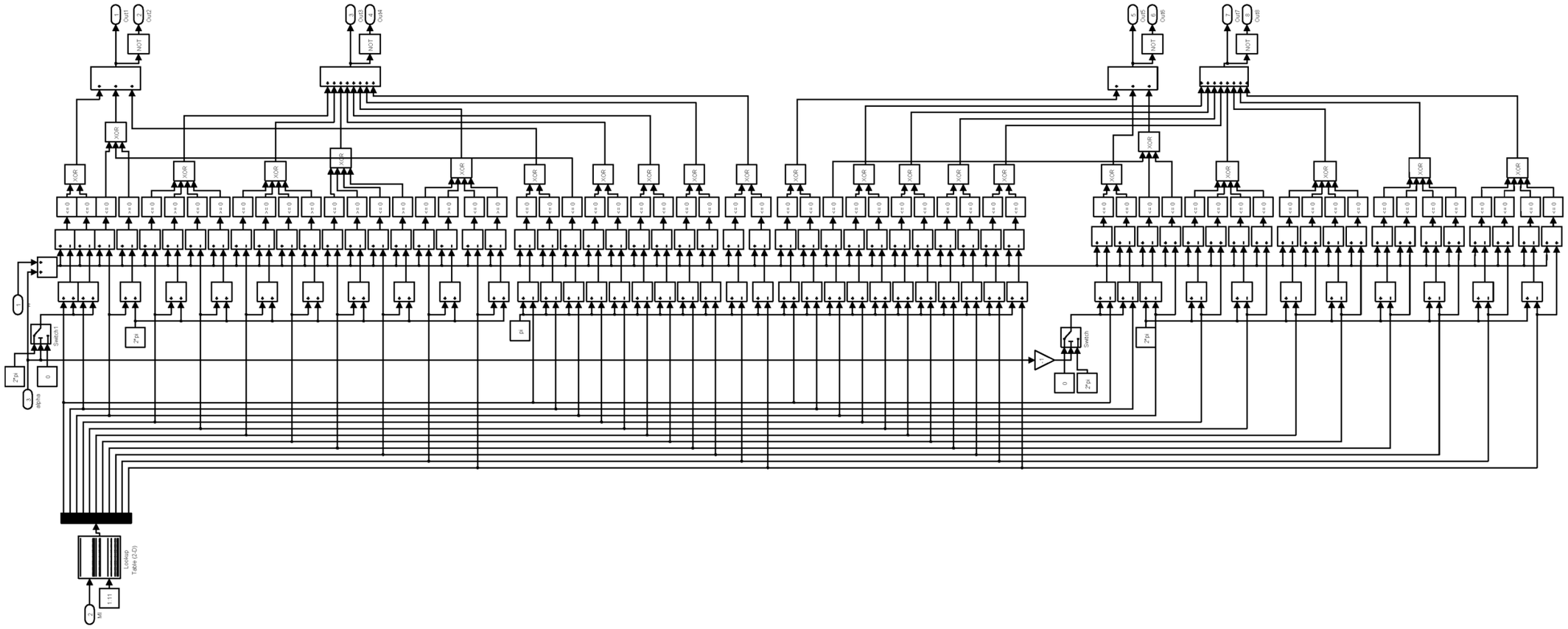


Figure K-3. Model of the “MSHE-PWM 3/8 with variable DC voltage-levels” block (i.e., red blocks shown in Figure K-2(a)).

Appendix L Five-Level CHI based STATCOM with The Associated Proposed Control Scheme and MSHE-PWM N = 3/8 with Variable DC Voltage-Levels Technique

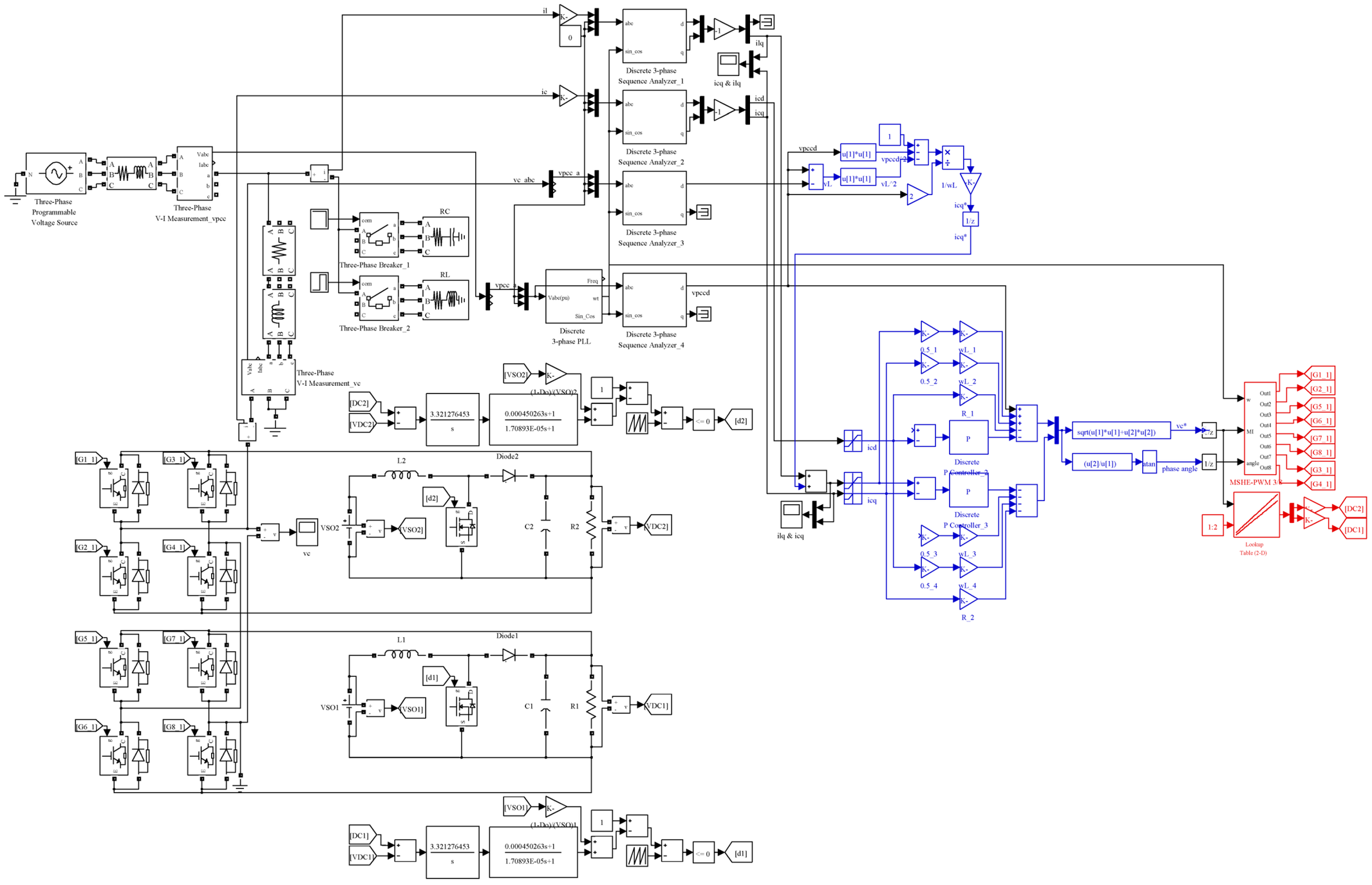


Figure L-1. Model of five-level CHI based single-phase STATCOM controlled by the associated proposed control scheme and MSHE-PWM 3/8 with variable DC voltage-levels technique.

Appendix M Three-phase Five-Level CHI based STATCOM with The Associated Proposed Control Scheme and MSHE-PWM *N* = 3/5 with Variable DC Voltage-Levels Technique

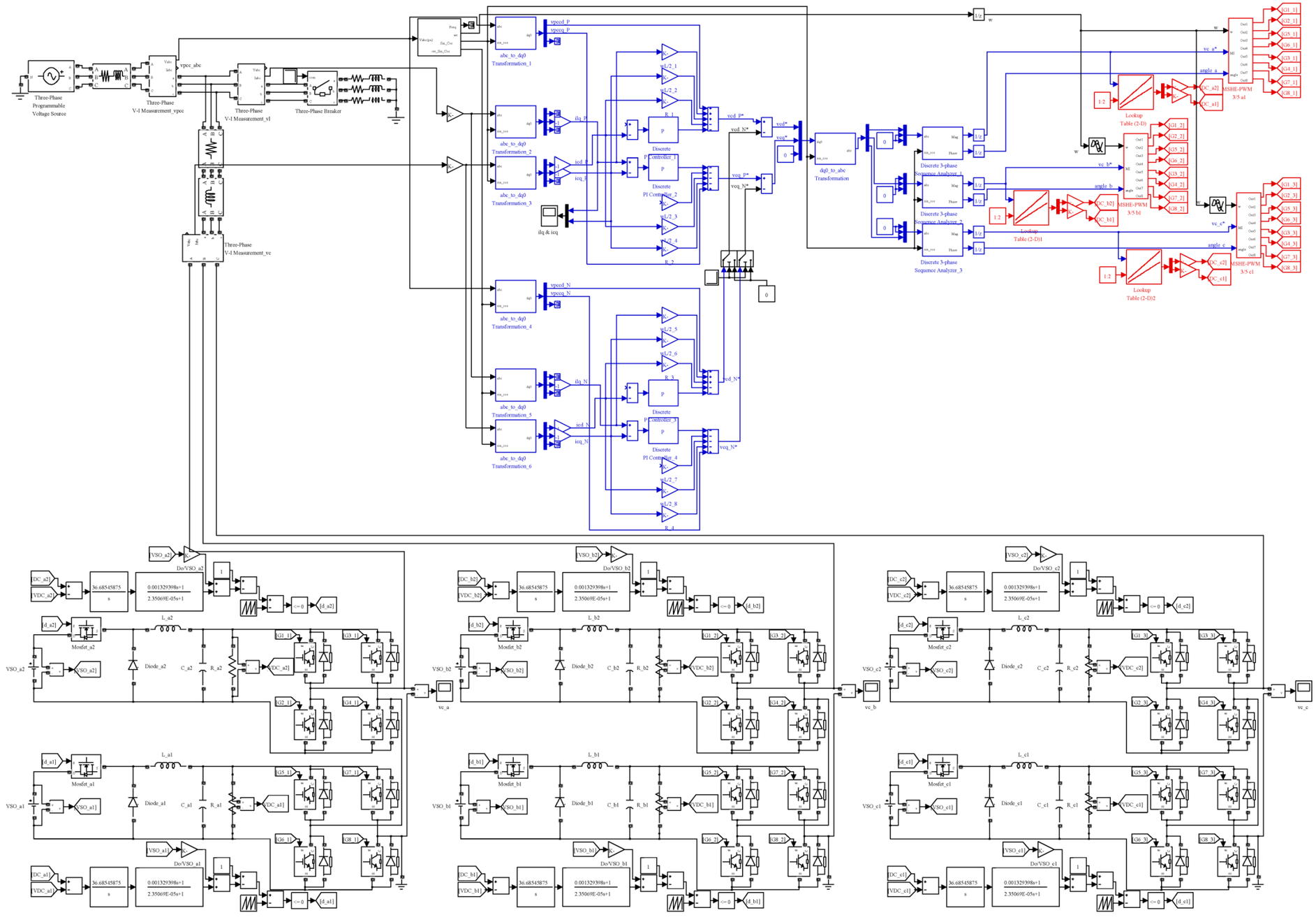


Figure M-1. Model of three-phase five-level CHI based single-phase STATCOM controlled by the associated proposed control scheme and MSHE-PWM 3/5 with variable DC voltage-levels technique under unbalanced load condition.